JW3311 Series

8/9/10 Cell Battery Protectors

Parameters Subject to Change Without Notice

DESCRIPTION

JW®3311 is a multi-cell battery protection IC that includes high-accuracy voltage detection circuits and delay circuits. It is possible for users to monitor the status of 8~10 series cell lithium-ion rechargeable battery pack.

JW3311 provides multiple protect functions including over-charge, over-discharge, over-current, over-temperature and open wire detection. More JW3311s can operate in cascade to protect long string battery.

FEATURES

- Wide range of operation voltage 6V to 60V
- Monitor 8~10 series cell battery and support cascaded operation
- High-accuracy voltage detection for each cell
  - Over-charge detection voltage V_{OC}: 3.6~4.4V (50mV step) ±20mV
  - Over-charge release hysteresis V_{OCRH}: 0.1~0.4V (100mV step)
  - Over discharge detection voltage V_{OD}: 2.3~3.0V (100mV step) ±80mV
  - Over-discharge release hysteresis V_{ODRH}: 0.2~0.5V (100mV step)
- Charge over-current detection four options 10 mV, 20 mV, 50 mV, Disable
- Discharge over-current detection in 3-step
  - 1st detection voltage V_{DOI1}: 0.05~0.2V (50mV step) ±10mV
  - 2nd detection voltage V_{DOI2}: $2V_{DOI1}$ (100mV step) ±20mV
  - Short circuit detection voltage V_{SHT}: 0.4~0.7V (100mV step) ±80mV
- High-accuracy battery temperature detection
  - Charging over-temperature protection threshold V_{COT}: 0.85V (50°C) ±30mV (±4°C)
  - Charging under-temperature protection threshold V_{CUT}: 0.23V (-10°C) ±30mV (±4°C)
  - Discharging over-temperature protection threshold V_{DOT}: 0.98V (70°C) ±25mV (±4°C)
- Three-step discharge over-current protection
  - For 1st, programmable from 0.1~10s
  - For 2nd, two options available (by part number)
    - (0.1~10s)×1%,
    - (0.1~10s)×10%
  - For 3rd, short circuit 300µs.
- Discharge disable mode selectable
- Open wire detection
- Charging Permission (CP) condition check
- Wide range of operation temperature -40°C to +85°C
- Low current consumption

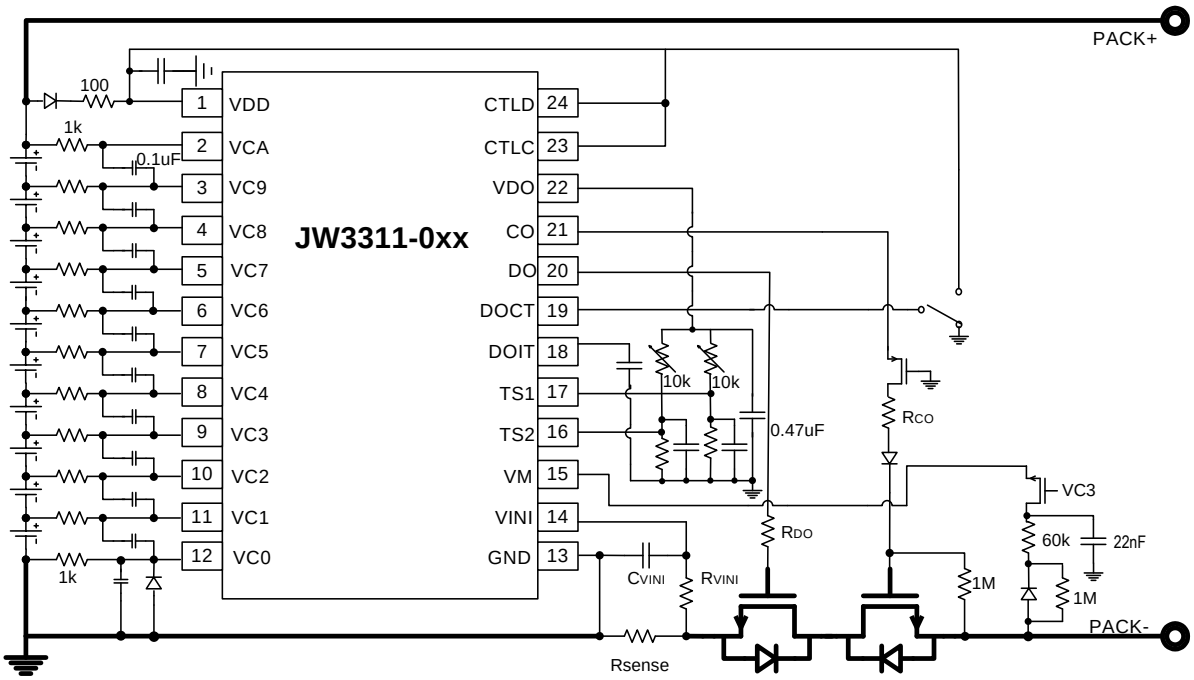
  Full power mode 20µA Max. (T=25°C)
  Sleep mode 13µA Max. (T=25°C)
  Shutdown mode 350nA Max. (T=25°C)
- Package: 24-Pin TSSOP

APPLICATIONS

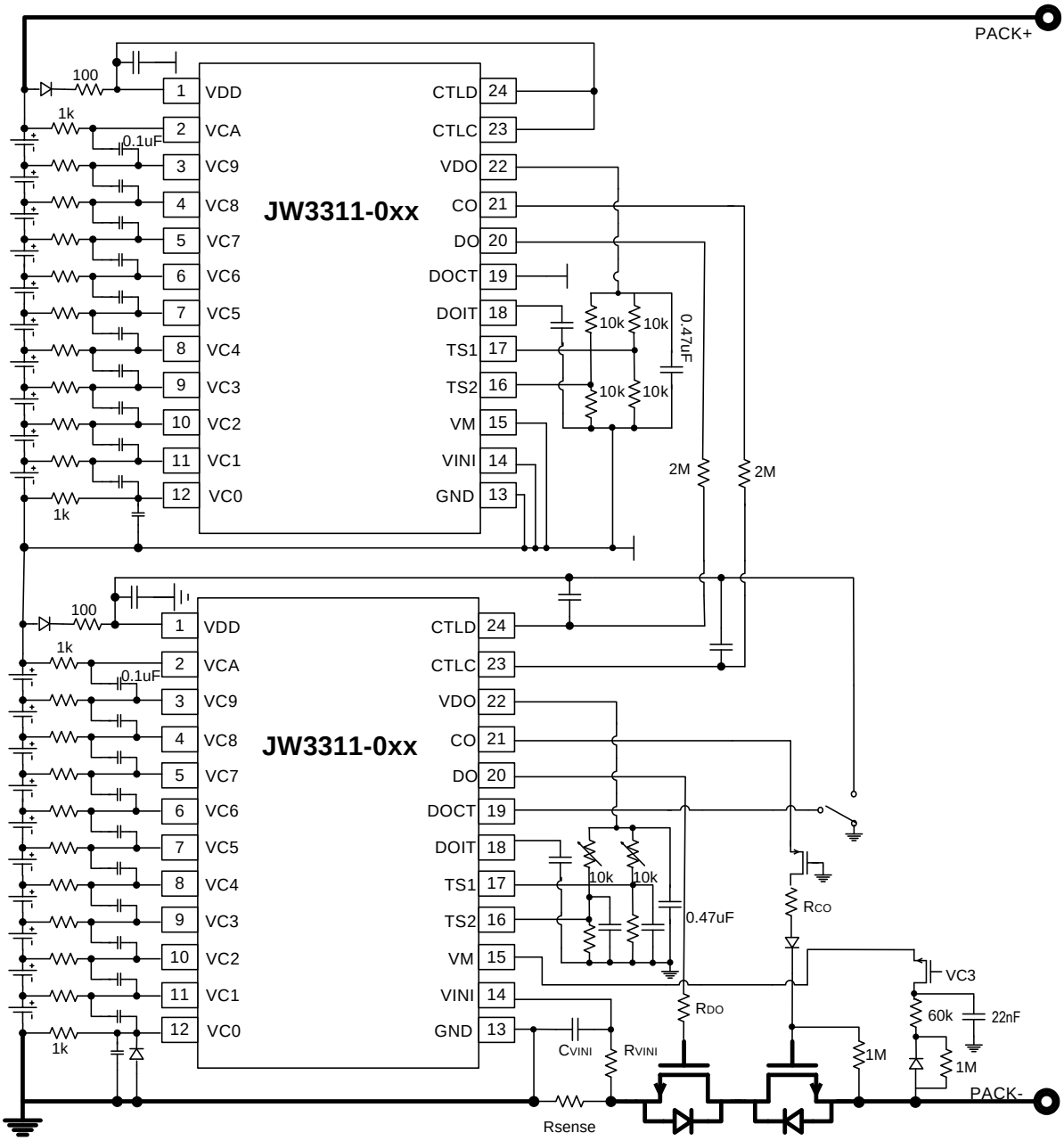
- Rechargeable lithium-ion battery pack
- Electric bicycles
- Motorcycles
- Backup battery systems
- Hybrid electric vehicles

TYPICAL APPLICATION

Single-stage operation (10cells)



Cascaded operation (20cells)



Remark: *when the cell11~cell20 had over-discharge fault, the load lock function is disabled. If need the load lock function, please refer to "User Manual"*

Selection Guides

Production name structure

JW3311-XXX

Series code*[1]
Sequentially set from AA to ZZ

Digital code*[2]
Sequentially set from 8, 9 and 0

1: Product Series List, relates to different detection threshold voltage

2. Battery No. Selection: 8→8Cells, 9→9Cells, 0→10Cells

Products Series List

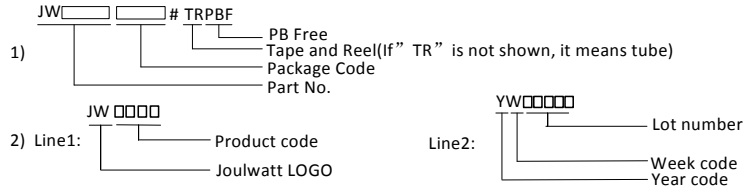
Type/Item	Over -charge detection voltage [V_{OC}]	Over -charge release voltage [V_{OCL}]	Over -discharge detection voltage [V_{OD}]	Over -discharge release voltage [V_{ODH}]	Charge over -current detection voltage [V_{COI}]	Discharge over-current 1 detection voltage [V_{DOI1}]	Discharge over-current 2 detection voltage [V_{DOI2}]	Short circuit detection voltage [V_{SHT}]	The Ratio of t_{doi2} and t_{doi1} [t_{doi2}/t_{doi1}]
JW3311-0NF	4.25V	4.15V	2.8V	3.0V	Disable	100mV	200mV	400mV	1%
JW3311-8NF	4.25V	4.15V	2.8V	3.0V	Disable	100mV	200mV	400mV	1%
JW3311-0HF	4.25V	4.15V	2.8V	3.0V	30mV	100mV	200mV	400mV	1%
JW3311-0AR	4.2V	4.1V	2.8V	3.0V	Disable	100mV	200mV	400mV	1%
JW3311-8AR	4.2V	4.1V	2.8V	3.0V	Disable	100mV	200mV	400mV	1%
JW3311-0HW	4.22V	4.12V	2.7V	3.0V	20mV	100mV	200mV	500mV	1%
JW3311-0AY	4.22V	4.12V	2.7V	3.0V	Disable	100mV	200mV	400mV	1%
JW3311-0AD	4.25V	4.15V	2.7V	3.0V	Disable	100mV	200mV	500mV	1%
JW3311-0AP	3.8V	3.5V	2.3V	2.6V	Disable	100mV	200mV	400mV	1%

Remark: *Please contact our sales office for products with detection voltage values other than those specified above.*

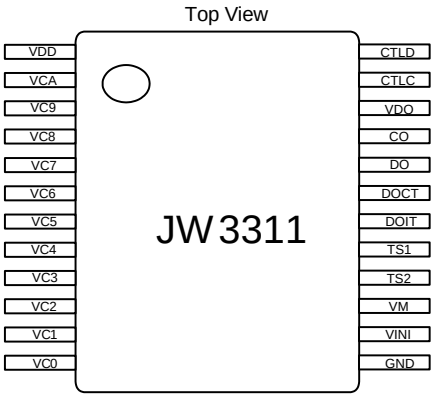
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW3311-0NFTSSOPC#TRPBF	TSSOP24	JW3311-0NF YW□□□□□
JW3311-8NFTSSOPC#TRPBF	TSSOP24	JW3311-8NF YW□□□□□
JW3311-0HFTSSOPC#TRPBF	TSSOP24	JW3311-0HF YW□□□□□
JW3311-0ARTSSOPC#TRPBF	TSSOP24	JW3311-0AR YW□□□□□
JW3311-8ARTSSOPC#TRPBF	TSSOP24	JW3311-8AR YW□□□□□
JW3311-0HWTSSOPC#TRPBF	TSSOP24	JW3311-0HW YW□□□□□
JW3311-0AYTSSOPC#TRPBF	TSSOP24	JW3311-0AY YW□□□□□
JW3311-0ADTSSOPC#TRPBF	TSSOP24	JW3311-0AD YW□□□□□
JW3311-0APTSSOPC#TRPBF	TSSOP24	JW3311-0AP YW□□□□□

Note：



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VDD,DOCT.....-0.3V~+60V
CTLD,CTLC.....VDD-5V~VDD+0.7V
VC0, VC1.....-0.3V~+24V
VC(n), n=2, 3, 4, 5.....-0.3V~+40V
VC(n), n=6, 7, 8, 9, A.....-0.3V~+60V
VM.....-0.3V~+24V
CO,DO.....-0.3V~+24V
VC(n)-VC(n-1).....-0.3V~20V
VCA..... (VDD-5V) to (VDD+0.3V)
VDO,TS1,TS2,DOIT,VINI..... -0.3V~+6.5V
Junction Temperature[2)]..... 150ºC
Lead Temperature 260ºC
Storage Temperature .....-65 ºC to +150 ºC

RECOMMENDED OPERATING CONDITIONS

B(N)-B(N-1).....0V to 5V
Junction Temperature (T_J) ..... -40ºC to 125ºC

THERMAL PERFORMANCE[3)]

	θ_{JA}	θ_{JC}
TSSOP24	42	9ºC/W

Note:

1) Exceeding these ratings may damage the device.

2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

TA = 25ºC, unless otherwise stated.

Item		Symbol	Condition	Min.	Typ.	Max.	Units
Power supply							
Operation voltage between VDD pin and GND pin		V_{DSOP}		6		60	V
Power-on reset threshold		V_{PON}			5.4	6	V
Shutdown threshold		V_{PDOWN}		4.7	5	5.3	V
Current consumption during full power		I_{FP}				20	μA
Current consumption during sleep		I_{SLEEP}				13	μA
Current consumption during shutdown		I_{SD}				350	nA
Detection period time for over-voltage and under-voltage		t_{DETV} [4]			0.4		s
Detection period time for discharge over-temperature		$t_{DISDETT}$ [4]			1.6		s
Detection period time for charge over-temperature/under-temperature		$t_{CHGDETT}$ [4]			3.2		s
Voltage/Current/Temperature Protections							
Over-charge	Protection threshold	V_{OC}		V_{OC}-0.020	V_{OC}	V_{OC}+0.020	V
	Release threshold	V_{OCL}		V_{OCL}-0.06	V_{OCL}	V_{OCL}+0.06	V
	Protection delay time	t_{OC} [4]		0.65	1	1.95	s
Over-discharge	Protection threshold	V_{OD}		V_{OD}-0.08	V_{OD}	V_{OD}+0.08	V
	Release threshold	V_{ODH}		V_{ODH}-0.12	V_{ODH}	V_{ODH}+0.12	V
	Protection delay time	t_{OD} [4]		0.65	1	1.95	s
Charge over-current	Protection threshold	V_{COI}	10mV	V_{COI}-5	V_{COI}	V_{COI}+5	mV
			20 mV / 50mV	V_{COI}-10	V_{COI}	V_{COI}+10	mV
	Protection delay time	t_{COI} [4]		270	540	810	ms
Discharge over-current	1st protection voltage	V_{DOI1}		V_{DOI1}-10	V_{DOI1}	V_{DOI1}+10	mV
	1st protection delay time	t_{DOI1} [4]	C_{DOIT} =4.7nF ±10%	390	780	1170	ms
		t_{DOI1S} [4]	DOIT pin short to GND	5	10	15	s
		t_{DOI1O} [4]	DOIT pin open	0.05	0.1	0.15	s
	2nd protection voltage	V_{DOI2}		V_{DOI2}-20	V_{DOI2}	V_{DOI2}+20	mV

	2st protection delay time	t_{DOI2} 4)	C_{DOIT} =4.7nF ±10% t_{DOI2}= t_{DOI1}×1%	3.9	7.8	11.7	ms
	Short protection voltage	V_{SHT}		V_{SHT}-80	V_{SHT}	V_{SHT}+80	mV
	Short protection delay time	t_{SHT} 4)		150	300	450	μs
Charge temperature protection	Over-temperature protection threshold	V_{COT}	50°C±4°C R_{NTC}=103AT	67.7%	70.6 %	73.3%	V_{VDOH}
	Over-temperature release hysteresis	V_{COTRH}	5°C		50		mV
	Under-temperature protection threshold	V_{CUT}	-10°C±4°C R_{NTC}=103AT	16.3%	19.1 %	22.2%	V_{VDOH}
	Under-temperature release hysteresis	V_{CUTRH}	5°C		40		mV
	Temperature protection delay time	t_{COT} 4)		2.4	3.5	6.7	s
Discharge temperature protection	Over-temperature protection threshold	V_{DOT}	70°C±4°C R_{NTC}=103AT	80%	81.8 %	83.4%	V_{VDOH}
	Over-temperature release hysteresis	V_{DOTRH}	5°C		30		mV
	Temperature protection delay time	t_{DOT} 4)		2.4	3.5	8.8	s
State detection	Discharge detection threshold	V_{TH_DSG}		1	3	5	mV
	Charge detection threshold	V_{TH_CG}		-5	-3	-1	mV
Input Voltage							
DOCT pin switching threshold		V_{DOCT}		3.5	3.9	4.3	V
DOCT detection delay time		t_{DOCT} 4)			225		ms
CTLD/CTLC sink current		I_{CTL}		0.8	1	1.5	μA
CTLD/CTLC sink current Hysteresis		I_{CTLH}			0.5		μA
CTLD/CTLC input voltage L		V_{CTLL}				V_{DD}-1.5	V
CTLD/CTLC input voltage H		V_{CTLH}		V_{DD}-0.5			V
Output Voltage							
VDO pin output voltage L		V_{VDOL}			0		V
VDO pin output voltage H		V_{VDOH}		1.15	1.2	1.25	V

VDO pin output current limit	V_{VDOI}		0.7	1	1.3	mA
CO output voltage L	V_{COL}		0		0.5	V
CO output voltage H	V_{COH}	Normal mode		12		V
		Sleep mode		10		V
DO output voltage L	V_{DOL}		0		0.5	V
DO output voltage H	V_{DOH}			12		V
Input Current						
VCA~VC0 pin current	I_{VC}		-1.0	0	1.0	μA
Output Current						
CO pin maximum source current	I_{COH}			8		mA
CO pin maximum sink current	I_{COL}			85		mA
DO pin maximum source current	I_{DOH}			8		mA
DO pin maximum sink current	I_{DOL}			85		mA
Load Detection						
Resistance between VM pin and GND pin	R_{VM}			125		kΩ
Load detection threshold	V_{VMD}		0.8	1	1.2	V
Charger Detection						
Charger detection pull up current	I_{PU}		0.8	1	1.2	μA
Charger detection threshold	V_{VMC}		2.5	3	3.5	V
Charging Permission Protection						
Single cell charging permission voltage	V_{CP}		0.7	0.9	1.1	V

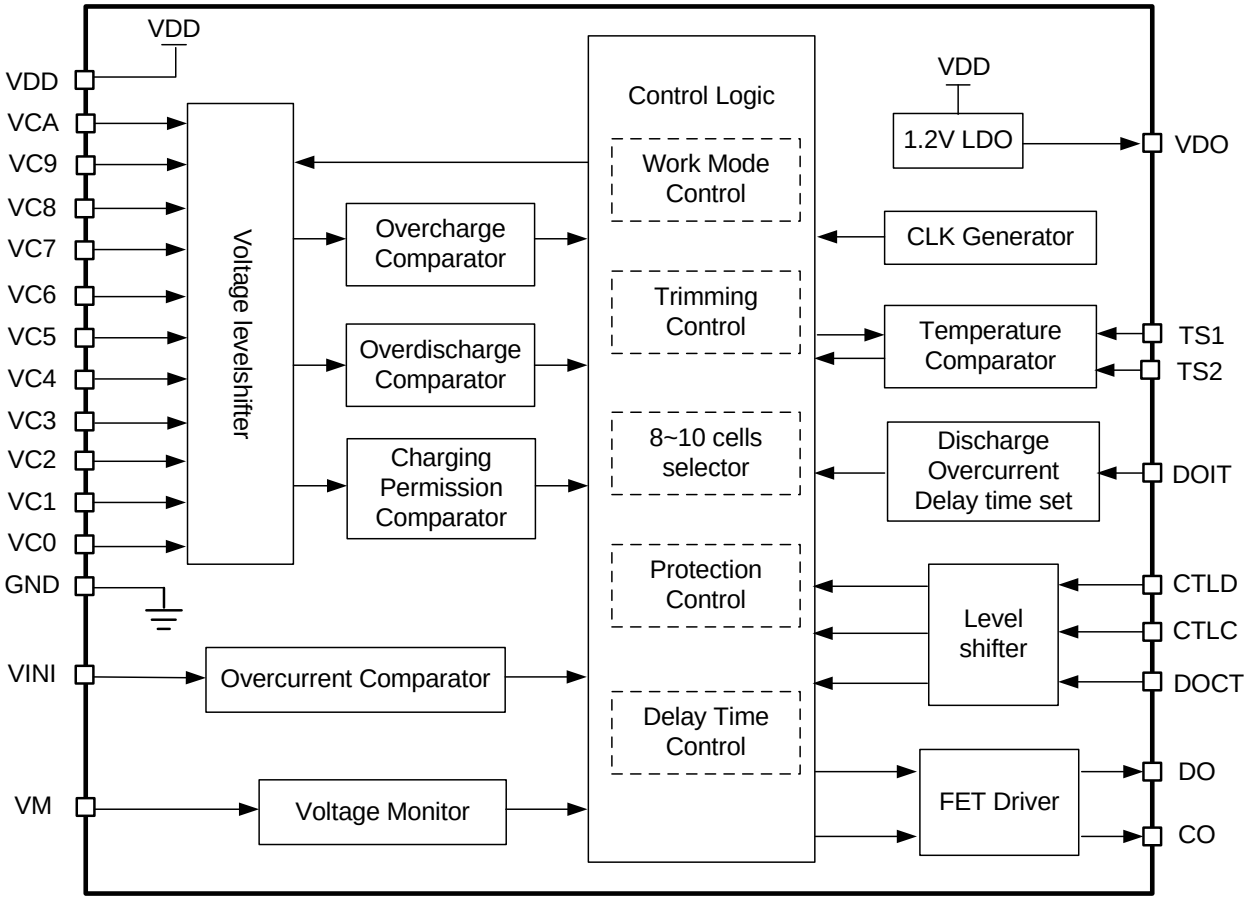
Note:

4) Guaranteed by design.

PIN DESCRIPTION

PIN No.	PIN Name	PIN Description
1	VDD	Input pin for positive power supply,
2	VCA	Connection pin for battery 10's positive voltage
3	VC9	Connection pin for battery 9's positive voltage
4	VC8	Connection pin for battery 8's positive voltage
5	VC7	Connection pin for battery 7's positive voltage
6	VC6	Connection pin for battery 6's positive voltage
7	VC5	Connection pin for battery 5's positive voltage
8	VC4	Connection pin for battery 4's positive voltage
9	VC3	Connection pin for battery 3's positive voltage
10	VC2	Connection pin for battery 2's positive voltage
11	VC1	Connection pin for battery 1's positive voltage
12	VC0	Connection pin for battery 1's negative voltage
13	GND	Input pin for negative power supply
14	VINI	Charge and discharge over-current detection terminal
15	VM	Load detection pin
16	TS2	Thermal sense input 2
17	TS1	Thermal sense input 1
18	DOIT	Discharge over-current delay time setting pin
19	DOCT	Pin for independently controlling discharge MOSFET
20	DO	Gate connection pin for discharge control MOSFET
21	CO	Gate connection pin for charge control MOSFET
22	VDO	1.2V LDO output. Must be bypass to GND with a 0.47μF ceramic capacitor for stable operation.
23	CTLC	CO controller for cascade application
24	CTLD	DO controller for cascade application

BLOCK DIAGRAM



OPERATION

Normal Status

In the JW3311, both CO and DO pins output high level voltage when all battery voltages are between V_{OD} and V_{OC}, the battery temperature is between V_{COT} and V_{CUT}, and the VINI pin voltage is less than V_{DOI1}. This is the normal status.

Over-charge Status

JW3311 detects cell voltage once per t_{DETV}. When any battery voltage increases to V_{OC} or more for longer than t_{OC}, the CO pin outputs low level voltage. Since the CO pin pulled down to the PACK- voltage by an external resistor, the charge MOSFET is turned off to stop charging. This is the over-charge status.

The over-charge status is released if either of the conditions mentioned below is satisfied:

(1) All battery voltage drops to V_{OCL} or less.

(2) The VINI pin voltage is higher than V_{TH_DSG} and all battery voltage drops to V_{OC}.

Over-discharge Status

JW3311 detects cell voltage once per t_{DETV}. When any voltage of batteries decreases to V_{OD} or lower for longer than t_{OD}, the DO pin outputs low level voltage. The discharge MOSFET is turned off and discharge stops. This is the over-discharge status. After entering to over-discharge status, the CO pin will output 10V to reduce power dissipation.

The VM pin is pulled down to the GND level via R_{VMS} internally.

The over-discharge status is released if either of conditions mentioned below is satisfied:

(1) The VM pin voltage is lower than V_{VMD}, and all battery voltages increase to V_{ODH} or more.

(2) The VM pin voltage is lower than V_{VMD}, and the VINI pin voltage is lower than V_{TH_CG} during charging.

Charge Over-current Status

In the JW3311, if the VINI pin voltage increases to V_{COI} or more for longer than t_{COI}, the CO and DO pins output low level voltage. The charge and discharge MOSFETs are turned off. This is the charge over-current status.

The VM pin is pulled up to the 5V level via I_{PU} internally.

The charge over-current status is released if the following condition is satisfied:

The VM pin voltage is higher than V_{VMC}

Discharge Over-current Status

In the JW3311, if the VINI pin voltage increases to V_{DOI} or more (discharge over-current threshold voltage) for longer than t_{DOI} (discharge over-current detection delay time), the DO pin outputs low level voltage. The discharge MOSFET is turned off and discharge stops. This is the discharge over-current status.

The VM pin is pulled down to the GND level via R_{VMS} internally.

JW3311 has three thresholds for discharge over-current detection (V_{DOI1}, V_{DOI2}, V_{SHT}).

The discharge over-current status is released if the following condition is satisfied:

The VM pin voltage is lower than V_{VMD}.

Delay Time Setting

In the discharge over-current detection, users are able to set the delay time through an external capacitor.

When the VINI pin voltage reaches V_{DOI1} or more, JW3311 starts charging C_{DOIT} (the DOIT pin capacitor) via I_{DOIT} (the DOIT pin output current). After a certain period, the DO pin outputs low level voltage. This period is t_{DOI1}, which can be calculated using the following equation.

$t_{DOI1}[s] = R_{DOI1}[\Omega] \times C_{DOIT}[nF]$

$=1.67\times10^{8}[\Omega] \times C_{DOIT}[nF]$

In case C_{DOIT}=4.7nF, t_{DOI1} is calculated as below.

$t_{DOI1}[s] = 1.67\times10^{8}[\Omega]\times 4.7\ [nF] = 0.785\ [s]$ (typ.)

The 2nd discharge over-current detection delay time (t_{DOI2}) is calculated as below.

$t_{DOI2}= t_{DOI1}\times1\%$ or $t_{DOI2}= t_{DOI1}\times10\%$

The ratio of t_{DOI2} and t_{DOI1} is 1% or 10% that could be selectable through part number.

The over-charge detection delay time, over -discharge detection delay time and load short circuit detection delay time are fixed internally.

Fault Detection on DOIT

To set the discharge over-current detection delay time, a capacitor is connected between DOIT pin and GND pin.

If the discharge over-current is detected and the DOIT pin is shorted to ground, t_{DOI1} is automatically changed to t_{DOI1S}.

In the same manner, if the discharge over-current is detected and the DOIT pin is floating, t_{DOI1} is automatically changed to t_{DOI1O}.

Battery Temperature Protection

JW3311 provides two temperature sensing pins (TS1&TS2) for detecting the temperature of battery cells. Two NTC (recommend 103AT, β=3435) resistors are placed nearby battery cells separately. JW3311 detects over-temperature or under-temperature once per t_{DETT} (temperature detection period time).

During temperature detection, only when VINI>V_{TH_DSG}, the JW3311 considers discharge state. Others, the JW3311 considers charge state.

In charge state, once the battery temperature is beyond V_{COT} or below V_{CUT}, JW3311 shuts down the charge MOSFET.

In charge stage, once the battery temperature is beyond V_{DOT}, JW3311 shuts down both charge and discharge MOSFETs. The discharging MOSFET turns on again till the temperature lower than V_{DOT}.

The charge temperature protection status is released if either of the following conditions is satisfied.

(1) The temperature of battery pack recovers

(2) The VINI pin voltage is higher than V_{TH_DSG}

In discharge state, once the battery temperature is beyond V_{DOT}, JW3311 shuts down both the charge and discharge MOSFETs. Till the temperature of battery pack recovers, the JW3311 turns on again the charge and discharge MOSFETs.

CTLD Pin and CTLC Pin

The CTLD/CTLC pins are used for cascaded operation. When any error is detected such as over-charge, over-discharge and temperature fault in the upper unit, the DO/CO pin signals are passed down to the CTLD/CTLC pins of the lower unit to control discharging/charging.

The status of output pins in abnormalities state detected is shown below table.

V_{CTLC}/V_{CTLD}(Input)		CO(Output)	DO(Output)
V_{CTLC}	VDD	H	H
	VDD-2	L	H
	Open	L	H
V_{CTLD}	VDD	H	H
	VDD-2	H	L
	Open	H	L

Discharge Disable Mode

The JW3311 provides discharge disable mode to independently control DO pin.

When the DOCT pins of all the units are connected to their respective GND pins, JW3311 works normally. If any of the DOCT pins is connected to the VDD pin, the DO pin voltage of the corresponding unit is forced to be low level voltage and this signal is passed down via the CTLD pin. As a result, JW3311 enters to the discharge disable mode and the discharge MOSFET is forced off. During this mode, only charging is enabled.

Then, by connecting all the DOCT pins back to the GND pins, JW3311 exits from this mode and meanwhile releases all the faults. Then JW3311 turns on both the charge/discharge MOSFETs for normal working.

Operation Modes

JW3311 has three power modes: Full Power mode, Sleep mode and Shutdown mode.

For Full Power mode, JW3311 detects over-voltage, under-voltage, over-temperature and under-temperature events in every detection period. Besides, over-current events are checked continuously. These safety events decide the status of the charge and discharge MOSFETs. The max current consumption is 20μA.

JW3311 enters Sleep mode after entering over-discharge status, temperature fault status or open wire status. During the sleep mode, the max current consumption is as low as 13μA.

JW3311 enters Shutdown mode when VDD pin voltage becomes lower than V_{PDOWN}. During this mode, JW3311 does not check for any safety events. Both the charge and discharge MOSFET are off. The max current consumption is as low as 350nA.

Open Wire Detection

JW3311 integrates open wire detection and protection. The open wire detection period is t_{OPEN}. When any of VC7 to VC1 pin is open, it detects open wire and charge and discharge is prohibited after a delay time.

The open wire protection is released when open wire point is connected again and the VM pin voltage is lower than V_{VMD}.

Charging Permission (CP) Protection

JW3311 provides charging permission function. If any battery cell voltage is lower than V_{CP}, JW3311 will enter to charge protection state.

When JW3311 enters to the CP protection state, the CO pin becomes 0V, turning OFF the charge MOSFET

Package and Bag Caution

1. JW3311-xxxx is Moisture-Sensitive Devices and its MSL[5)] (Moisture-Sensitive Level) is level-3.
2. Calculated shelf life in sealed bag is 12 months at <40℃ and <90%RH(Relative Humidity).
3. Peak package body temperature[5)] is 260℃.
4. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within 168 hours of factory at the condition ≤30℃/60%RH.

b) Stored at <10%RH.

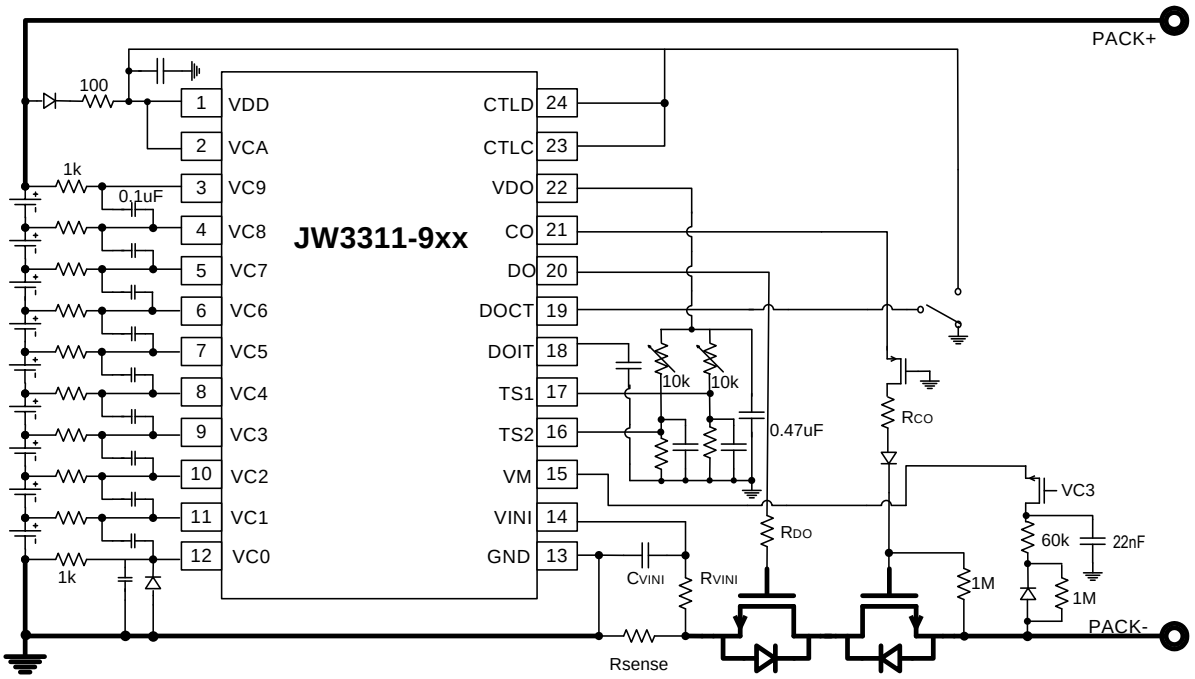
5. Devices require bake before mounting if Humidity Indicator Car(HIC) is >10%RH when read at 23±5℃.
6. If baking is required, devices may be baked for 48 hours at 125 ± 5 ℃. If device containers cannot be subjected to high temperature for shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure.

Note:

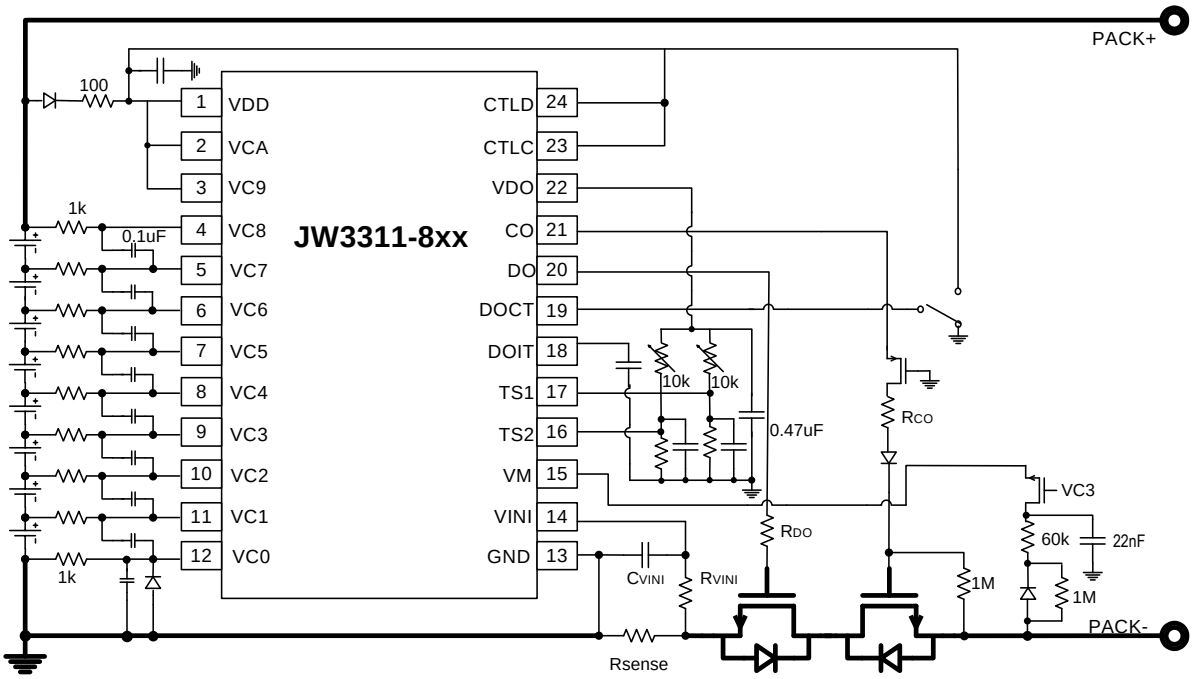
5) Level and body temperature defined by IPC/JEDEC J-STD-020.

REFERENCE DESIGN:

- Single-stage operation (9cells)

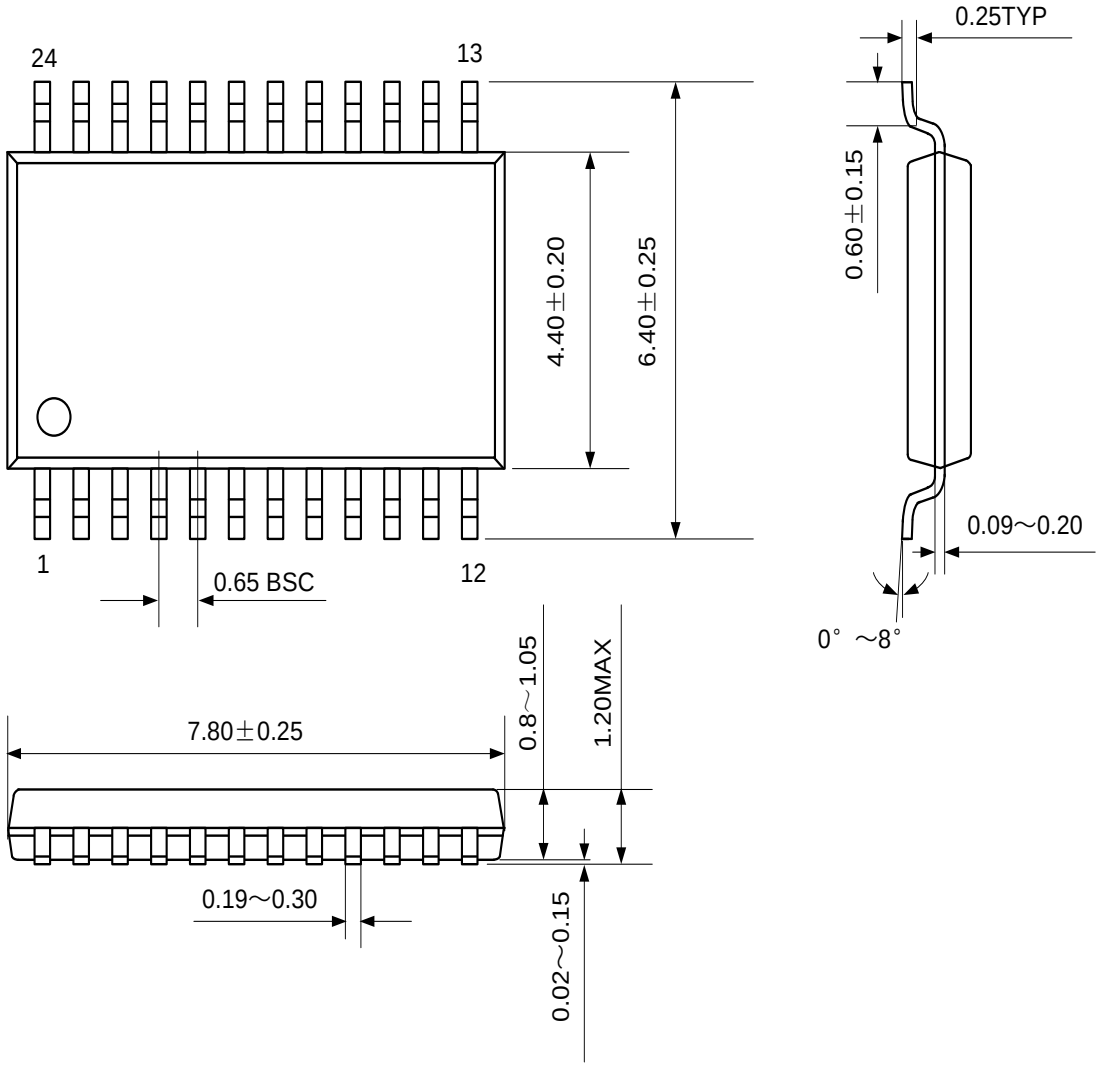


- Single-stage operation (8cells)



PACKAGE OUTLINE

TSSOP24 UNIT: mm



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