JW7222

Positive High-Voltage Hot Swap and Inrush Current Controller With Power Limiting

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®7222 is positive hot swap controller that allows a board to be safety inserted and removed from a live backplane or other hot power sources. JW7222 offers inrush current control to protect MOSFET against system voltage droop and transients. The function of power limit protection allows better utilization of the external MOSET's SOA. An external capacitor connected from TMR to GND establishes the timeout period to declare a fault condition and Gate is turned off when timeout. The POWER GOOD keeping high declares MOSFET is turned on. The under voltage threshold can be programmed via external resistor dividers.

JW7222 is available in a 10-pin MSOP package.

FEATURES

- Wide operating range: 2.5 V to 18 V
- Inrush current limit for safe board insertion into live power sources
- Programmable maximum power dissipation in the external pass device
- Accurate 26.5mV current-sense threshold
- Power good: active low
- Circuit breaker function for severe overcurrent events
- Internal high side charge pump and gate driver for external N-channel MOSFET
- Adjustable under-voltage lockout (UVLO) and hysteresis
- Drop-In upgrade for LTC4211/TPS24711-no layout
- 10-Pin MSOP package

APPLICATIONS

- Server Backplane Systems
- Storage Area Networks
- Plug-In Modules
- Medical Systems
- Base Stations

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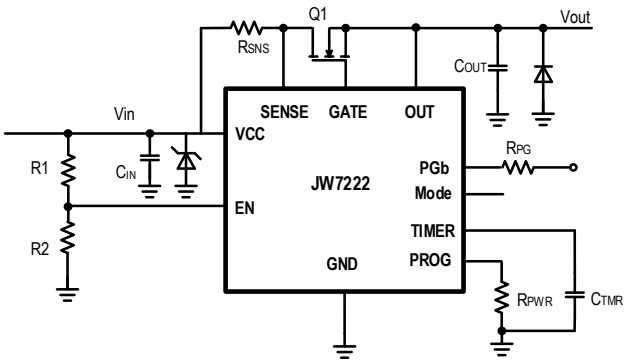
TYPICAL APPLICATION

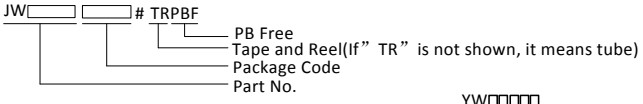


ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW7222MSOP#TRPBF	MSOP10	JW7222 YW□□□□□

Notes:

1)



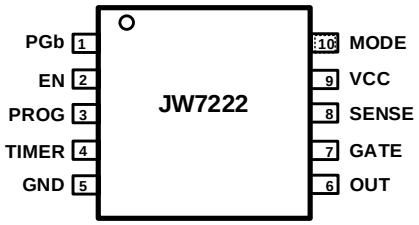
2)

DEVICE INFORMATION

DEVICE[1)]	PGb	Latch off/Retry
JW7222MSOP#TRPBF	Active Low	Retry

PINCONFIGURATION

TOP VIEW



MSOP10

ABSOLUTE MAXIMUM RATING[1)]

EN, MODE, OUT, PGb, GATE, SENSE, VCC ..... -0.3V to 30V
PROG Pin..... -0.3V to 3.6V
SENSE Pin to VCC Pin..... -0.3V to 0.3V
TIMER..... -0.3V to 5V
MODE, PGb sink current..... 5mA
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model) .....±2kV
ESD Susceptibility (Charged Device Model) .....±750V

RECOMMENDED OPERATING CONDITIONS[3)]

VCC, SENSE…….....2.5V to 18V
EN, MODE, PGb, OUT…….....……..…….……0 to 18V
PGb sink current……..…..……..... 2mA
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
MSOP10	166.5	41.8ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RESCOMMENDE OPERATING CONDITIONS

2) The JW7222 include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40~125ºC, EN=3V and RPROG=50kΩ to GND. unless otherwise stated.

Item	Symbol	Condition	Min.	Typ.	Max.	Units
INPUT (VCC PIN)						
UVLO rising threshold	$V_{CC\_UVLO\_H}$	VCC rising	2.2	2.32	2.45	V
UVLO falling threshold	$V_{CC\_UVLO\_L}$	VCC falling	2.1	2.22	2.35	V
UVLO hysteresis	$V_{CC\_UVLO\_HYST}$			100		mV
Supply current	I_Q	EN=3V $I_Q=I_{OUT}+I_{VCC}+I_{SENSE}$		1	1.2	mA
	I_{SHDN}	EN=0V $I_{SHDN}= I_{OUT}+I_{VCC}+I_{SENSE}$		0.9		mA
EN						
EN Threshold voltage, falling	$V_{EN\_Falling}$	EN falling	1.2	1.3	1.4	V
EN hysteresis	V_{EN_HYST}			50		mV
Input leakage current	I_{LEAK_EN}	$0 \le V_{EN} \le 30V$	-1	0	1	uA
MODE						
Mode switch threshold	V_{MDOE_SW}		1.2	1.35	1.5	V
PGb						
Threshold	V_{PGb_H}	$V_{(SENSE-OUT)}$rising, PGb going high	140	240	340	mV
Hysteresis	V_{PGb_HYST}	$V_{(SENSE-OUT)}$falling, PGb going low		70		mV
Output low voltage	V_{PG_PD}	Sinking 2 mA		0.11	0.25	V
Input leakage current	I_{LEAK_PGb}	V_{PGb}=0V, 30V	-1	0	1	uA
PROG						
Bias voltage	V_{PROG_BIAS}	Sourcing 10 uA	0.65	0.678	0.7	V
Input leakage current	I_{LEAK_PROG}	V_{PROG}=1.5V	-0.2	0	0.2	uA
TMR						
Sourcing current	I_{TMR_SRC}	V_{TIMER}=0V	8	10	12	uA
Sinking current	$I_{TMR\_SNK\_EN}$	V_{TIMER}=2V	8	10	12	uA
	$I_{TMR\_SNK\_DIS}$	V_{EN}=0V, V_{TIMER}=2V	2	4.5	7	mA
Upper threshold voltage	V_{TMR_UP}		1.3	1.35	1.4	V
Lower threshold voltage	V_{TMR_LOW}		0.33	0.35	0.37	V
Timer activation voltage	V_{TMR_ACT}	Raise Gate until I_{TIMER} sinking, measure $V_{(GATE-VCC)}$,VCC=12V	5	5.9	7	V
Bleed-down resistance	R_{TMR_BLD}	V_{EN}=0V, V_{TMR}=2V	70	104	130	kΩ
OUT						
Input bias current	I_{OUT_BIAS}	V_{OUT}=12V		45	90	uA
GATE						
Output voltage	V_{GATE}	V_{OUT}=12V	23.5	25.8	28	V
Clamp voltage	V_{GS}	Inject 10uA into GATE, measure	12	13.9	15.5	V

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V_{CC} = 12V, T_J = -40~125ºC, EN=3V and RPROG=50kΩ to GND. unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
		$V_{(GATE-VCC)}$				
Sourcing current	I_{GATE_SRC}	V_{GATE}=12V	20	30	40	uA
Sinking current	$I_{GATE\_SNK\_FST}$	Fast turn off, V_{GATE}=14V	0.5	1	1.4	A
	I_{GATE_SNK}	Sustained, V_{GATE}=4 to 23V	6	11	20	mA
	I_{GATE_INRSH}	In inrush current limit, V_{GATE}=4V to 23V	20	30	40	uA
Pulldown resistance	R_{GATE_PD}	Thermal shutdown	14	20	26	kΩ
SENSE						
Input bias current	I_{SNS_BIAS}	V_{SENSE}=12V		30	40	uA
Current limit threshold	V_{SNS_LMT}	V_{OUT}=12V	24	26.5	29	mV
		V_{OUT} =0.5V MODE=0V		1.5		mV
Power limit threshold	$V_{SNS\_LMT\_7V}$	V_{OUT} =7V, R_{PROG}=50kΩ	10.1	11.6	13.1	mV
	$V_{SNS\_LMT\_2V}$	V_{OUT} =2V, R_{PROG}=25kΩ	10.1	11.6	13.1	mV
	$V_{SNS\_LMT\_3mV}$	V_{OUT} =2.23V, R_{PROG}=82kΩ	1.5	3	4.5	mV
Fast-trip threshold	V_{SNS_FST}		35	40	45	mV
OTSD（Over Temperature Shut Down）						
Shutdown temperature[5)]	T_{SD}	Temperature rising	130	140		℃
Shutdown temperature Hysteresis[5)]	T_{SD_HYST}			10		℃
EN Timing Requirements						
Turn off time	t_{EN_off}	EN↓ to V_{GATE}-V_{OUT}<1V,C_{GATE}=33nF	20	35	50	us
Deglitch time	t_{EN_DGLH}	EN↑	8	14	18	us
Disable delay	t_{off_delay}	EN↓ to GATE↓， C_{GATE}=0. $t_{pff50-90}$ See Figure1	0.1	0.4	1	us
PGb Timing Requirements						
Deglitch time	t_{delay_PGb}	Rising or falling edge	2	3.4	6	ms
GATE Timing Requirements						
Fast turn off duration	t_{off_FST}		8	13.5	18	us
Turn on delay	t_{delay_on}	Vcc ↑ to GATE sourcing, $t_{prr50-50}$, See Figure 2		1.8	2.3	ms
SENSE Timing Requirements						
Fast-turnoff duration	t_{SNS_off}		8	13.5	18	us
Fast-turnoff delay	t_{SNS_delay}	$V_{(VCC-SENSE)}$=80mV, C_{GATE}=0pF, Tprf50-50, See Figure 3		200		ns

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Note：

5) Guaranteed by design.

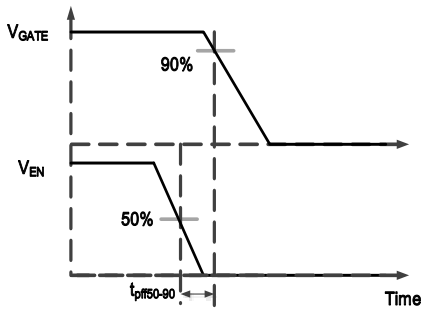

Figure 1. $t_{pff50-90}$ Timming Definition

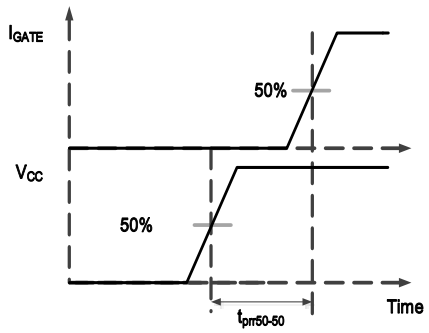

Figure 2. $t_{prr50-50}$ Timming Definition

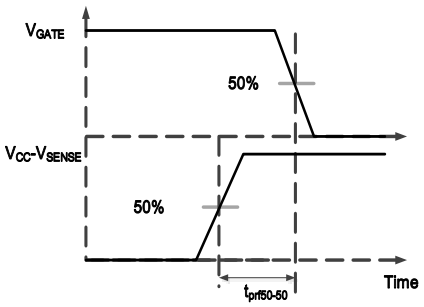

Figure 3. $t_{prr50-50}$ Timming Definition

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PIN DESCRIPTION

JW7222 MSOP-10	Name	Description
1	PGb	Active-low, open-drain power good indicator. Status is determined by the voltage across the MOSFET.
2	EN	Active-high enable input. Logic input.
3	PROG	Power-limiting programming pin. A resistor from this pin to GND sets the maximum power dissipation for the FET.
4	TIMER	A capacitor connected from this pin to GND to program fault timing period.
5	GND	Ground
6	OUT	Output voltage sensor for monitoring MOSFET power.
7	GATE	Gate driver output for external MOSFET
8	SENSE	Current sensing input for resistor shunt from VCC to SENSE.
9	VCC	Input-voltage sense and power supply
10	MODE	Pull to GND: Current limit fold back to 1.5mV when V_{OUT}<1V Pull high or floating: Current limit fold back function is disabled. Power limit protection still works.

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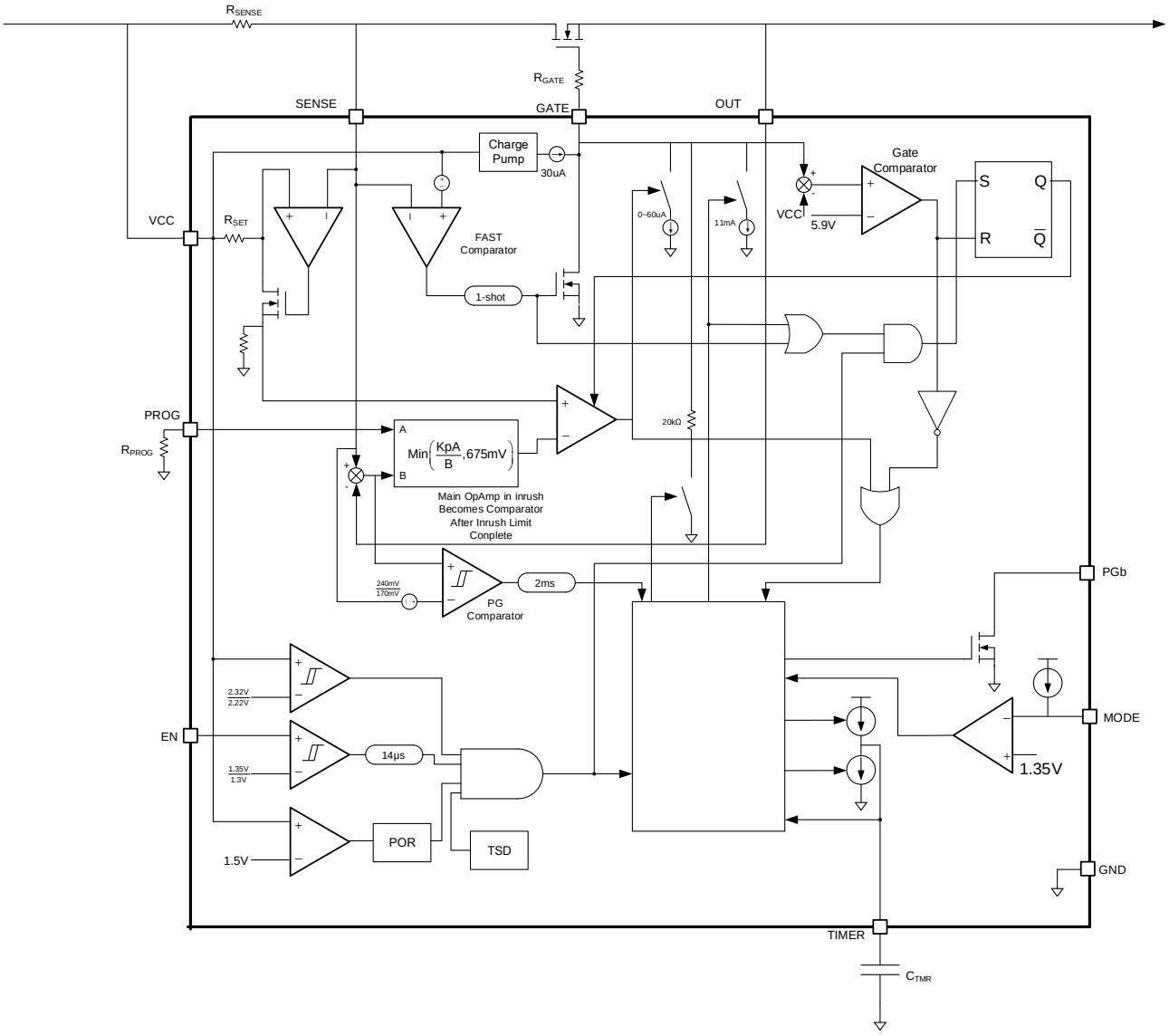
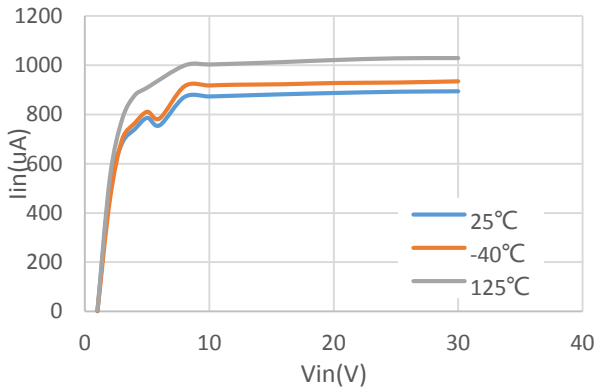
BLOCK DIAGRAM



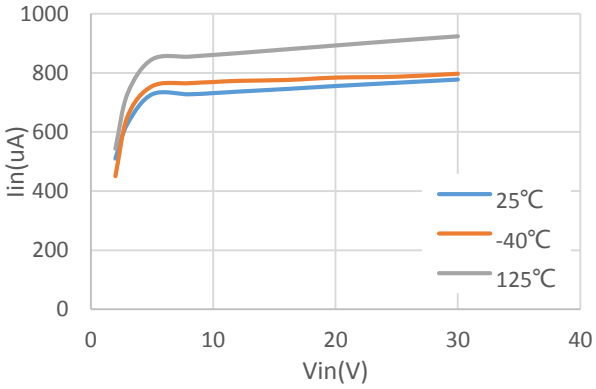
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted

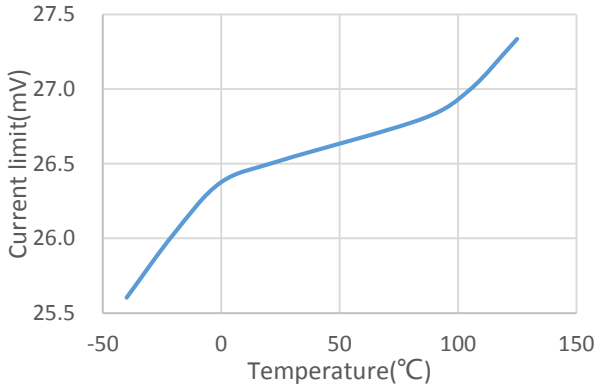
V_{IN} Supply Current Vs. Input Voltage



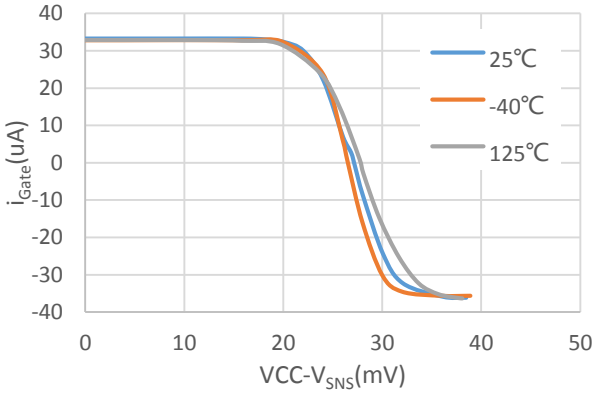
Shutdown Current Vs. Input Voltage



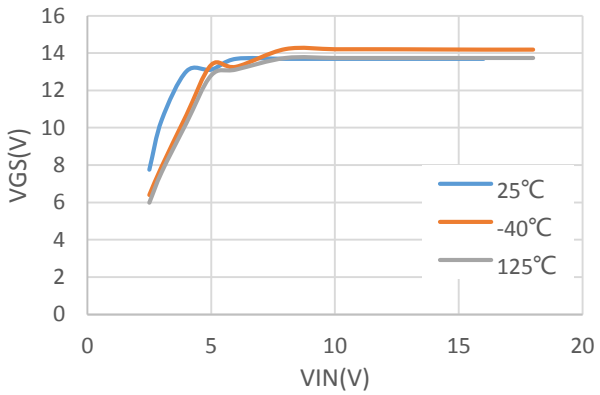
Current limit VS. Temperature



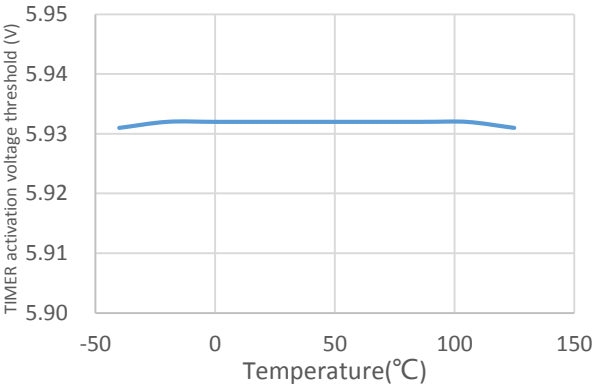
Gate Current VS. Voltage Across R_{SNS}



VGS With Zero Gate Current VS. Input Voltage



TIMER Activation Voltage Threshold VS. Temperature



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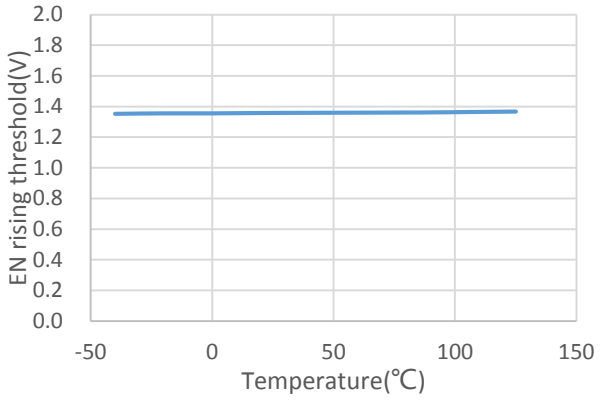
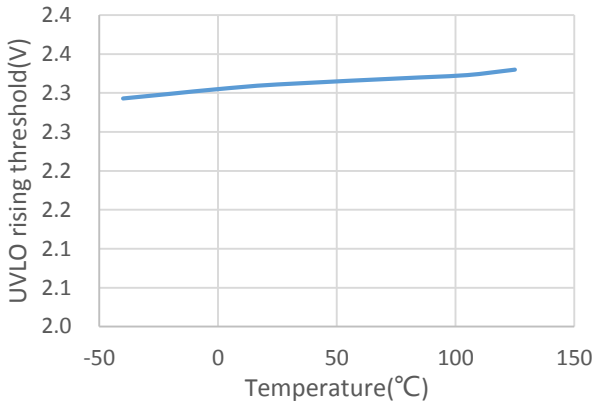
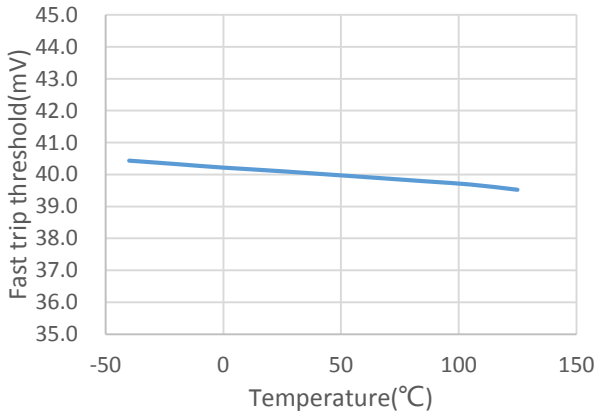
EN Rising Threshold VS. Temperature



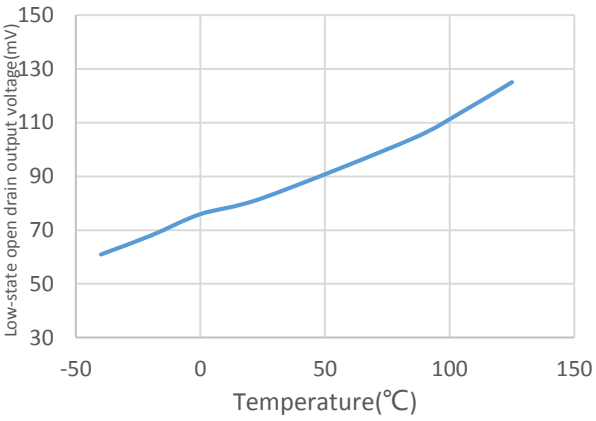
UVLO Rising Threshold VS. Temperature



Fast Trip Threshold VS. Temperature



PGb Open Drain Output Voltage in Low State



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FUNCTIONAL DESCRIPTION

The JW7222 is a hot swap controller that provide inrush current limit protection thereby allowing a board to be safely inserted and removed from a live backplane. Current limit and power limit protection prevent system against hot short circuit or power supply transient events.

Board Plug In

When hot-plug events happen, JW7222 is held inactive, for a short period (insertion time) until internal voltages stabilize. During this period, the gate of external N-channel MOSFET is pulled down by internal 11mA sink current. The 11mA pull down current prevents an inadvertent turn-on as the Miller capacitor of external MOSFET is charged. Also PROG and TIMER are held low and PGb is held open drain. After insertion time, Inrush time begins and GATE is sourced by 30uA if EN threshold was exceeded. The power dissipation of external MOSFET is detected by monitoring VDS and drain current. If MODE pin is pull down to GND, a 1.5mV fold back current limit loop works when Vout<1V. If MODE pin is pull up or float, fold back function is disabled.

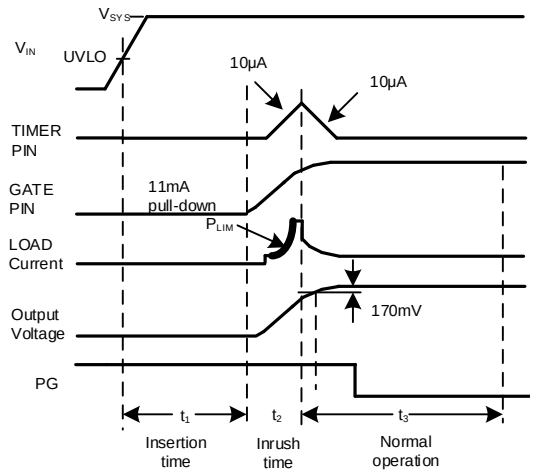


Figure 1. Power-Up Sequence

Inrush Operation

After insertion time and EN is active, the inrush time begins. During inrush time, the inrush current is limited by current limit or power limit protection.

Fold back current limit function can be enabled by connecting MODE pin to GND. If MODE pin is pull down to GND, a 1.5mV fold back current limit loop works when Vout<1V. If MODE pin is pull up or float, fold back function is disabled. An internal 10μA sourcing current charges CTMR while current limit or power limit protection is active. If the VGATE-VCC exceed the timer activation voltage (VTMR_ACTIVE =5.9 V for VCC = 12 V). The TIMER then begins to discharge CTMR with a current of approximately 10 μA and normal operation mode starts. If the VGATE-VCC is still below the timer activation voltage when the voltage of CTMR reaches 1.35V. A fault condition is declared and the external MOSFET is turned off. CTMR can be computed by below equation:

$$C_{TMR} \geq \frac{t_{inrush\_time} \times 10\mu A}{1.35V}$$

Action of the Constant-Power Engine

The power limit protection allows the better utilization of external MOSFET's SOA. In most cases, inrush current is limited by power limit function. The power limit protection is active only when VGATE-VCC is below the timer active voltage. The power dissipation is calculated by multiplying the VDS (VSNS-VOUT) of the external MOSFET and the voltage across RSNS. The power limit is programmed by the external resistor connected between PROG and GND. When the power limit is active, the GATE is modulated to regulate the power dissipation around power limit threshold. The power limit

program resistor (RPROG) can be calculated using following equation:

$$R_{PROG} = \frac{3125}{P_{LIM} \times R_{SENSE} + 0.9mV \times V_{CC\_MAX}}$$

Current Limit

The load current is measured by the voltage between VCC and SNS. JW7222 utilizes two current limit thresholds:

	Current Limit	Condition
I_{CL1}	26.5mV	$I_{CL1} \times V_{DS} < P_{LIM}$ & $V_{GATE}-V_{CC} < V_{TMR\_ACTIVE}$
I_{CL2}	1.5mV	MODE=0V & VOUT<1V & $V_{GATE}-V_{CC} < V_{TMR\_ACTIVE}$

The current limit protection is active when the voltage across the sense resistor R_{SNS} reaches I_{CL1}/I_{CL2}. In the current limit condition, the GATE is modulated to regulate the voltage across R_{SNS} around I_{CL1}/I_{CL2} and C_{TMR} is charged by internal 10μA sourcing current. If the load current decrease below I_{CL1}/I_{CL2} before the voltage of TIMER reaching 1.35V, IC entry to normal operation mode. The R_{SNS} resistor is recommended to be smaller than 100 mΩ.

Circuit Breaker and Fast Trip

The JW7222 monitors load current by sensing the voltage across RSNS. In normal operation mode (VGATE-VCC>VTMR_ACTIVE) the JW7222 incorporates two distinct thresholds: a current-limit threshold and a fast-trip threshold. When the current exceeds the current-limit threshold, CTMR is charged by 10μA current. If the voltage on CTMR reaches 1.35 V, then the external MOSFET is turned off. The JW7222 commences a restart cycle, as shown in Figure 2.

Overload between the current limit and the fast trip threshold is permitted in this period. This shutdown scheme is sometimes called an electronic circuit breaker. The fast-trip threshold protects the system against a severe overload or a dead short circuit. When the voltage across the sense resistor RSENSE exceeds the 40 mV fast-trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximately 1 A of current as shown in Figure 3. This extremely rapid shutdown may generate disruptive transients in the system, in which case a low-value resistor inserted between the GATE pin and the MOSFET gate can be used to moderate the turn off current. The fast-trip circuit holds the MOSFET off for only a few microseconds, after which the JW7222 turns back on slowly, allowing the current-limit feedback loop to take over the gate control of MOSFET Then the hot-swap circuit goes into auto-retry mode.

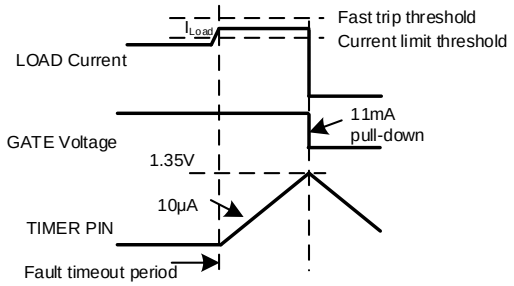


Figure 2. Current Limit Threshold

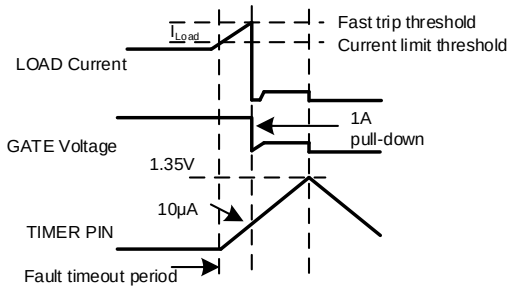


Figure 3. Fast Trip Threshold

Automatic Restart

The JW7222 enters automatic restart sequence. The TIMER pin continues to charge and discharge between 0.35V and 1.35V 15 times as shown in Figure 4. During restart sequence,

the C_{TMR} charging current is 10μA while discharging current is 10μA. When the TIMER pin reaches 0V during the 16th high to low ramp, the 30μA current sourcing at the GATE pin turns on external MOSFET. If the fault condition is not removed, the timeout period and the restart cycle repeat.

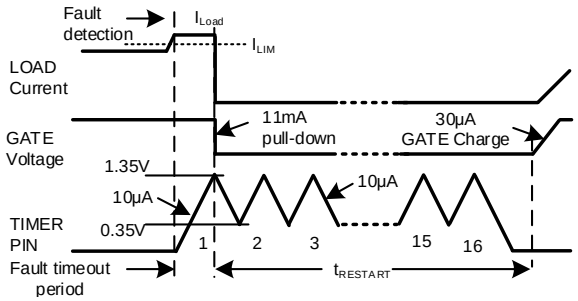


Figure 4. Restart Sequence

PGb and Timer Operations

The open-drain PGb output provides a deglitched end of inrush indication based on the voltage across MOSFET. PGb is useful for preventing a downstream dc/dc converter from starting while its input capacitor COUT is still charging. PGb goes active low about 3.4 ms after COUT is charged. This delay allows external MOSFET to fully turn on and any transients in the power circuits to end before the converter starts up. This type of sequencing prevents the downstream converter from demanding full current before the power-limiting engine allows the MOSFET to conduct the full current set by the current limit ILIM. Failure to observe this precaution may prevent the system from starting. The pullup resistor shown on the PGb pin in the typical application diagram on the front page is illustrative only; the actual connection to the converter depends on the application. The PGb pin may indicate that inrush has ended before the MOSFET is fully enhanced, but the downstream capacitor will have been charged to substantially its full operating voltage. Care should be taken to ensure that the MOSFET on-resistance is sufficiently small to ensure that the voltage drop across this transistor is less than the power-good threshold. After the hot-swap circuit successfully starts up, the PGb to high-impedance status whenever the drain-to-source voltage of MOSFET exceeds its upper threshold of 240 mV, which presents the downstream converters a warning flag. This flag may occur as a result of overload fault, output short fault, input overvoltage, higher die temperature, or the GATE shutdown by UVLO and EN.

The fault timer starts when a current of approximately 10 μA begins to flow into the external capacitor, CTMR, and ends when the voltage of CTMR reaches TIMER upper threshold. The fault-timer state requires an external capacitor CTMR connected between the TIMER pin and GND pin. The length of the fault timer is the charging time of CTMR from 0 V to its upper threshold of 1.35 V. The fault timer begins to count under any of the following three conditions:

1. In the inrush mode, TIMER begins to source current to the timer capacitor, CTMR, when MOSFET is enabled. TIMER begins to sink current from the timer capacitor, CTMR when V(GATE – VCC) exceeds the timer activation voltage (see the Inrush Operation section). If V(GATE – VCC) does not reach the timer activation voltage before TIMER reaches 1.35 V, then the JW7222 disables the external MOSFET. After the MOSFET turns off, the timer goes into retry mode.

2. In an overload fault, TIMER begins to source current to the timer capacitor CTMR, when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, CTMR, and the GATE pin is pulled to ground. After the fault timer period, TIMER goes into retry mode.

3. In output short-circuit fault, TIMER begins to source current to the timer capacitor, CTMR, when the load current exceeds the programmed current limits following a fast-trip shutdown of MOSFET. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor CTMR, and the

GATE pin is pulled to ground. After the fault timer period, TIMER goes into retry mode.

If the fault current drops below the programmed current limit within the fault timer period, VTIMER decreases and the pass MOSFET remains enabled. If the timer capacitor reaches the upper threshold of 1.35 V, then: TIMER charges and discharges CTMR between the lower threshold of 0.35 V and the upper threshold of 1.35 V for sixteen cycles before the JW7222 attempts to re-start. The TIMER pin is pulled to GND at the end of the 16th cycle of charging and discharging and then ramps from 0 V to 1.35 V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the IC is disabled by UVLO or EN.

Over Temperature Shutdown

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. IC implements a thermal sensing circuit to monitor the operating junction temperature. Once the die temperature rises to approximately +140℃ the thermal protection disable the gate driver and also causes the PGb pins to go to high-impedance states. Once the junction temperature drops to 130℃, the IC restart to work.

Start-Up of Hot-Swap Circuit by VCC or EN

The connection and disconnection between a load and the system bus are controlled by turning on and turning off the MOSFET. The JW7222 has two ways to turn on external MOSFET:

1. Increasing VCC above UVLO upper threshold while EN is already higher than its upper threshold sources current to the GATE pin. After an inrush period, JW7222 fully turns on external MOSFET.

2. Increasing EN above its upper threshold while VCC is already higher than UVLO upper threshold sources current to the GATE pin. After an inrush period, JW7222 fully turns on external MOSFET. The EN pin can be used to start up the JW7222 at a selected input voltage VCC. To isolate the load from the system bus, the GATE pin sinks current and pulls the gate of MOSFET low. The MOSFET can be disabled by any of the following conditions: UVLO, EN, load current above current limit threshold, hard short at load, or OTSD. Three separate conditions pull down the GATE pin:

1. GATE is pulled down by an 11-mA current source when any of the following occurs.

– The fault timer expires during an overload current fault (VSENSE > 26.5 mV).

– VEN is below its falling threshold.

– VCC drops below the UVLO threshold.

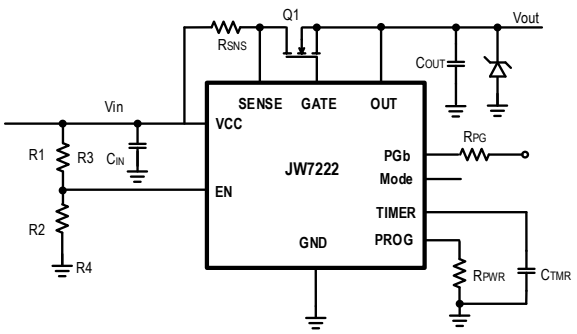
2. GATE is pulled down by a 1-A current source for 13.5 μs when a hard output short circuit occurs and V(VCC – SENSE) is greater than 40 mV, i.e., the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the external MOSFET remains off.

3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

APPLICATION INFORMATION

The JW7222 is hot swap controller for 2.5~18V system application and is used to manage inrush current and protect downstream circuitry and upstream bus in case of fault condition.

Typical Application



Design Requirements

The table below summarizes the design parameters that must be known before designing a hot swap circuit. Keeping load off until hot swap is fully powered up is recommended and it can be realized by using PG function. Starting load early causes unnecessary stress on external MOSFET and could lead to MOSFET failure to startup.

PARAMETER	VALUE
Input Voltage Range	10~14V
Maximum Load Current	10A
UVLO Rising Threshold	9V
C_{OUT}	470μF
Maximum Ambient Temperature	50ºC

R_{SNS} Selection

Before selecting R_{SNS}. First compute the maximum load current I_{max}. To provide some margin, set the target current I_{CL} to 1.2×Imax and compute R_{SNS} using equation below:

$$R_{SNS} = \frac{26.5mV}{1.2 \times I_{max}} = \frac{26.5mV}{1.2 \times 10A} = 2.2083m\Omega$$

Using next available R_{SNS} of 2mΩ. Current limit can be computed as 13.25A. In addition, if a precise current limit is desired, a sense resistor with a resistor divider can be used as shown in Figure 9.

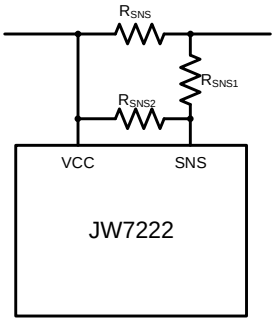


Figure 9. SENSE Resistor Divider

The current limit using resistor divider can be calculated as below equation:

$$i_{CL} = \frac{26.5mV}{R_{SNS}\frac{R_{SNS2}}{R_{SNS1}+R_{SNS2}}}$$

The R_{SNS1} is recommended to be smaller than 10Ω.

External MOSFET Selection

The JW7222 drives an external N-channel MOSFET to limit inrush current and protect system from fault condition such as over current, under voltage and over temperature. The important features of the MOSFETs are R_{DSON}, the maximum drain-source voltage and the SOA. Device with V_{GS} lower than 12V rating can be used if a Zener diode is connected. Sufficient $V_{DS(MAX)}$ margin is recommended because the MOSFET may experience much higher transient voltages during extreme conditions. A MOSFET with a $V_{DS(MAX)}$ rating of at least twice the maximum input supply voltage is recommended.

The next factor need to consider is $R_{DS(ON)}$, The

maximum voltage droop across MOSFET should be less than power good threshold 70mV.

$$R_{DS(ON)} \leq \frac{70mV}{12A} = 5.83m\Omega$$

Taking these factors into consideration, the IRLS3813PbF is selected for this example. The MOSFET has a maximum gate-source rating of 20V. and maximum $R_{DS(ON)}$ of 1.95mΩ. The $R_{\theta JC}$ is 0.64 ºC/W while $R_{\theta JA}$ is 40 ºC/W.

The effect of R_{DSON} upon the maximum operating temperature should be considered by following equation.

$$R_{DS(ON)} \leq \frac{T_{J\_MAX} - T_{A\_MAX}}{{I_{MAX}}^2 \times R_{\theta JA}} = \frac{130 - 50}{12^2 \times 40} = 13.9m\Omega$$

Power Limit Selection

In general, the power limit P_{LIM} of the JW7222 should be set to prevent the die temperature from exceeding a short-term maximum temperature T_{JMAX} of the MOSFET. Usually T_{JMAX} of the MOSFET could be set as 130. Leave some margin to usual manufacture's rating 150ºC. P_{LIM} can be set by following equation:

$$P_{LIM} \leq \frac{T_{J\_MAX} - ({I_{MAX}}^2 \times R_{DS(ON)} \times R_{\theta CA} + T_{A\_MAX})}{R_{\theta JC}} = \frac{130 - (12^2 \times 0.00195 \times 40 + 50)}{0.64} = 107W$$

$V_{SNS\_PL\_MIN}$ is the minimum sense voltage during power limit operation. Usually $V_{SNS\_PL\_MIN}$ is measured when drain-source voltage is max. Due to offsets of internal amplifiers, programmed power limit (P_{LIM}) accuracy degrades at low $V_{SNS\_PL\_MIN}$ and could cause start-up issues. To ensure reliable operation, verify that $V_{SNS\_PL\_MIN} \geqslant 1.5mV$ using below equation

$$V_{SNS\_PL\_MIN} = \frac{P_{LIM} \times R_{SNS}}{V_{CC\_MAX}}$$

Therefore, the P_{LIM} should be larger than 10.5W. Take this factors into consideration, P_{LIM} is set as 40W. The maximum power dissipation of the external MOSFET can be programmed by an external resistor R_{PROG}. The value of R_{PROG} can be computed by following equation.

$$R_{PROG} = \frac{3125}{P_{LIM} \times R_{SNS} + 0.9mV \times V_{CC\_MAX}}$$

R_{PROG} can be computed as 33.7kΩ for this example. The next available value is 33kΩ.

C_{TMR} Selection

The fault timeout time should be larger than the maximum output voltage rise time. It is critical to keep downstream DC/DC converter off while the hot swap is charging bulk capacitor. If the $P_{LIM}<I_{LIM}\times V_{CC\_MAX}$ and MODE is float or pulled up. the estimated startup time can be computed by following equation:

$$t_{start} = \frac{C_{OUT}}{2} \times \left(\frac{{V_{CC\_MAX}}^2}{P_{LIM}} + \frac{P_{LIM}}{{I_{LIM}}^2}\right)$$

If the $P_{LIM}<I_{LIM}\times V_{CC\_MAX}$ and MODE is connected to GND. the estimated startup time can be computed by following equation:

$$t_{start} = \frac{C_{OUT}}{2} \times \left(\frac{\left(V_{CC\_MAX} - 1V\right)^2}{P_{LIM}} + \frac{P_{LIM}}{{I_{LIM}}^2}\right) + \frac{C_{OUT} \times 1V \times R_{SNS}}{1.5mV}$$

If the $P_{LIM}>I_{LIM}\times V_{CC\_MAX}$, the startup time can be calculated by below equation:

$$t_{start} = \frac{C_{OUT} \times V_{CC\_MAX}}{I_{LIM}}$$

The next step is to determine the minimum fault-timer period. t_{start} is output voltage rising

time, some additional time must be added to the charge time to account for additional gate voltage rise. The fault timer (t_{FLT}) continues to run until VGS rises 5.9V(for V_{CC}=12V) above input voltage. t_{FLT} can be compute as equation below

$$t_{FLT} = t_{start} + \frac{5.9V \times C_{ISS}}{I_{GATE}}$$

For this application, P_{LIM}<I_{LIM}×V_{CC_MAX} and MODE is connected to GND, the t_{start} can be estimated as 1.245ms and tFLT can be estimated as 2.818ms. To ensure that fault timeout cannot be triggered during inrush time, 50% fault timeout margin is recommended. C_{TMR} can be computed with following equation.

$$C_{TMR} = \frac{t_{FLT} \times 10\mu A}{1.35V} = \frac{150\% \times 2.818ms \times 10\mu A}{1.35V}$$

The next available C_{TMR} is chosen as 33nF. The t_{FLT} can be calculated by below equation:

$$t_{FLT} = \frac{C_{TMR} \times 1.35V}{10\mu A} = \frac{33nF \times 1.35V}{10\mu A} = 4.465ms$$

UVLO Setting

UVLO threshold can be programmed by external resistor divider. Usually the rising UVLO threshold should be set sufficiently below the minimum input voltage For this example, UV rising threshold is 9V. The UVLO threshold can be calculated by below equation

$$V_{UVLO\_rising} = \frac{R_2 + R_1}{R_2} \times 1.35V$$

Assume R_1 is 100kΩ, R_2 can be computed by equation shown as

$$R_2 = \frac{R_1}{\frac{V_{UVLO\_rising}}{1.35V} - 1} = 17.6k\Omega$$

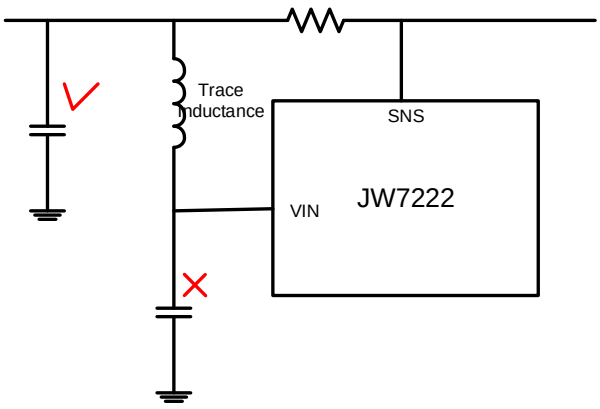
Final Schematic and Component Values

PARAMETER	VALUE
R_{SNS}	2mΩ
R_1	100kΩ
R_2	17.6kΩ
R_{PROG}	33kΩ
dQ_1	IRLS3813PbF
C_{TMR}	33nF
C_{OUT}	470μF

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. VCC pin and SNS pin need to have a Kelvin Sense connection to the sense resistor R_{SNS}.
2. Keep the decoupling capacitor on VCC pin as close to the IC as possible.
3. A Shottky diode is recommended to be connected From GND to OUT pin.
4. A large voltage can develop between VCC and SNS, if the bypass capacitor is placed right next to the pin and the trace from R_{SNS} to the pin is long, a LC filter is formed. This could result in a violation of the ABS max rating from VCC to SNS.



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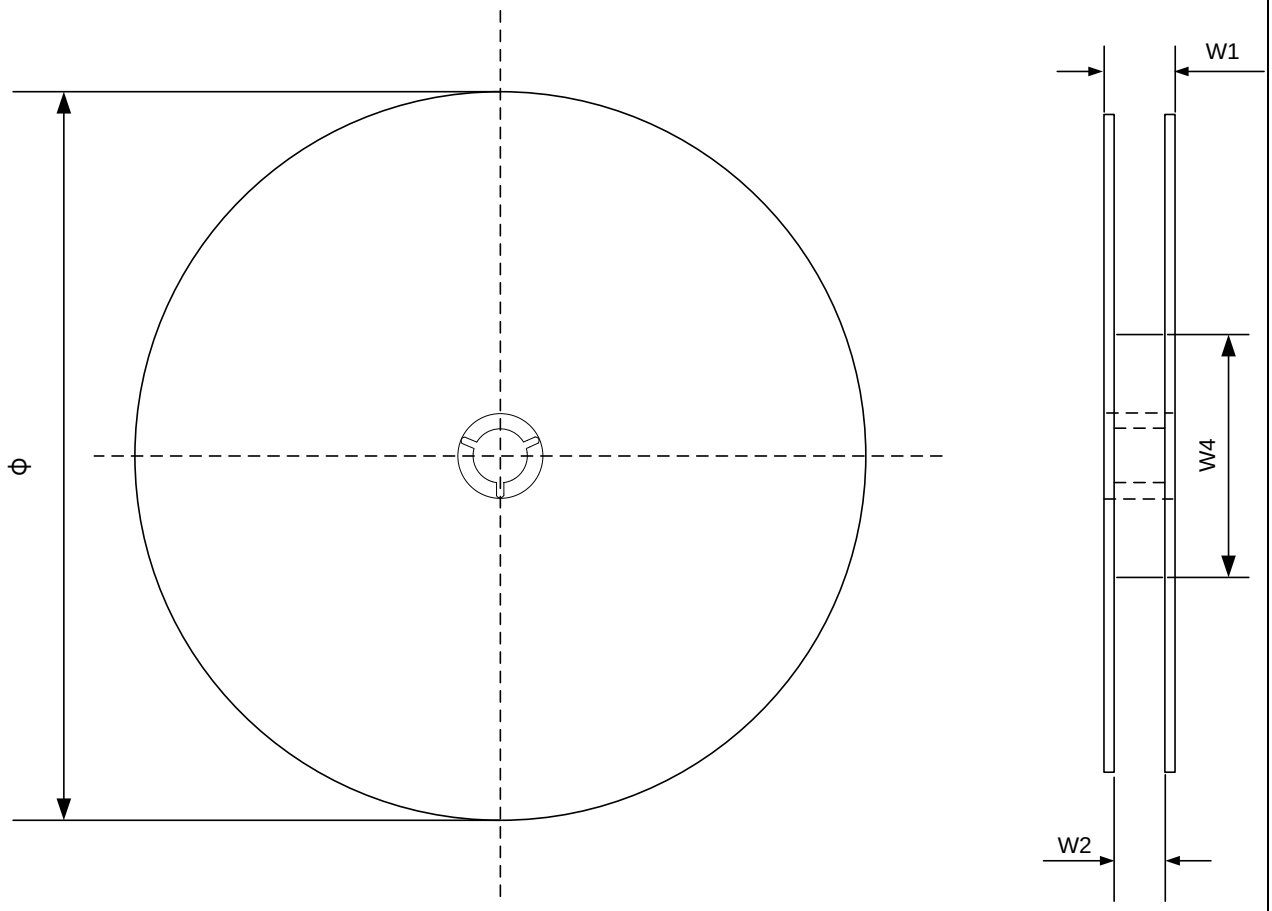
TAPE AND REEL INFORMATION

Reel UNIT: mm



Package	Diameter Φ	Thickness W1	Width W2	W4
MSOP10	330±2	17.6±2	12.4±2	100±2

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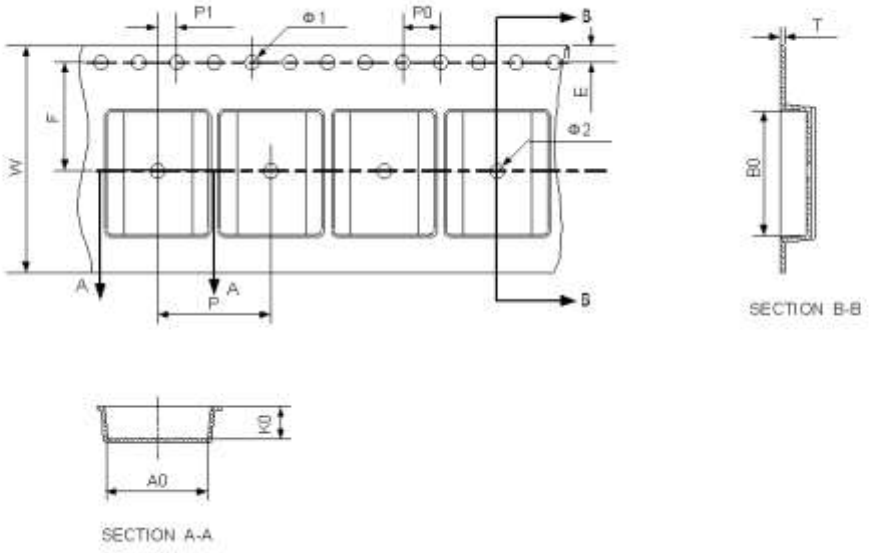
Carrier Tape UNIT: mm



Package	P0	P1	P	A0	B0	W	T0	K0	Φ1	Φ2	E	F
MSOP10	4.0±0.1	2.0±0.05	8.0±0.1	5.2±0.1	3.3±0.1	12	0.25±0.02	1.2max	1.5	1.5	1.75±0.1	5.50±0.05

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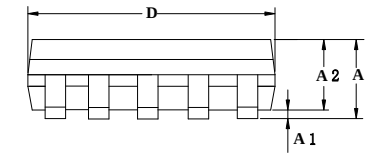
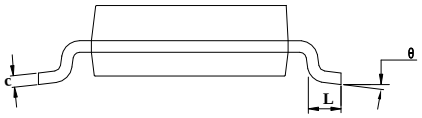
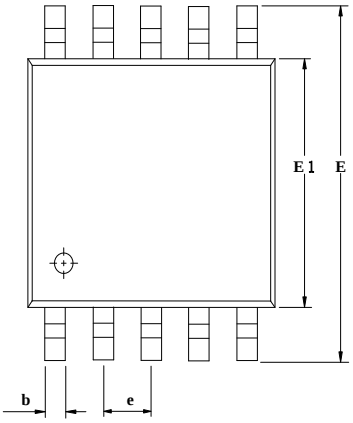
PACKAGE OUTLINE

MSOP10 UNIT: mm

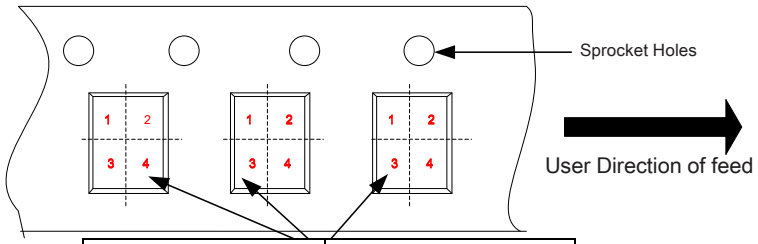






Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.02	—	0.15
A2	0.75	—	0.95
b	0.18	—	0.33
c	0.09	—	0.23
D	2.90	3.00	3.10
E	4.75	—	5.05
E1	2.90	—	3.10
e	0.50(BSC)		
L	0.40	—	0.80
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package	Pin1 Quadrant
MSOP10	1

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