JW7221/JW7221L

Positive High-Voltage Hot Swap and Inrush Current Controller With Power Limiting

DESCRIPTION

The JW®7221 and JW®7221L are positive hot swap controllers that allows a board to be safely inserted and removed from a live backplane or other hot power sources. JW7221/W7221L offers inrush current control to protect MOSFET against system voltage droop and transients. The function of power limit protection allows better utilization of the external MOSFET's SOA. An external capacitor connected from TMR to GND establishes the timeout period to declare a fault condition and Gate is turned off when timeout condition occurs. The POWER GOOD keeping high declares MOSFET is turned on. The under voltage and over voltage protection threshold can be programmed via external resistor dividers. The JW7221L provide latch off mode after a fault condition occurs while JW7221 provide automatically restart mode.

JW7221 and JW7221L are available in a 10-pin MSOP package.

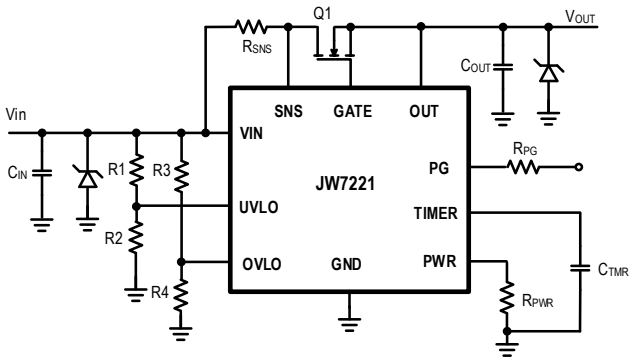
FEATURES

- Wide operating range: 9 V to 80 V
- Inrush current limit protection
- Programmable power limit
- Adjustable current limit: 55mV±11%
- Circuit breaker function for severe overcurrent events
- Internal high side charge pump and gate driver for external N-channel MOSFET
- Adjustable under-voltage lockout (UVLO) and hysteresis
- Adjustable over-voltage lockout (OVLO) and hysteresis
- Initial insertion timer allows ringing and transients to subside after system connection
- Programmable fault timer
- Active high open drain power good output
- Available in latched fault and automatic restart versions
- 10-Pin MSOP package

APPLICATIONS

- Server Backplane Systems
- Base Station Power Distribution Systems
- Solid State Circuit Breaker
- 24-V and 48-V Industrial Systems

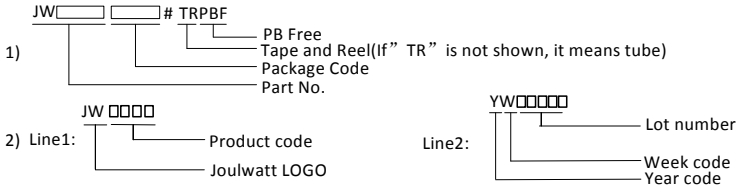
TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW7221MSOP#TRPBF	MSOP10	JW7221 YW□□□□□
JW7221LMSOP#TRPBF	MSOP10	JW7221L YW□□□□□

Notes：

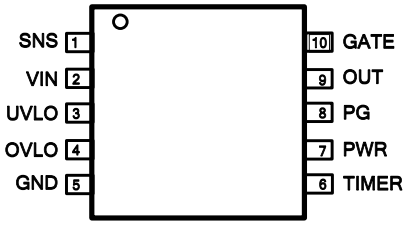


DEVICE INFORMATION

DEVICE[1)]	FEATURE	STATUS
JW7221MSOP#TRPBF	Auto-recovery protection mode	Available
JW7221LMSOP#TRPBF	Latch-off protection mode	Contact the factory

PINCONFIGURATION

TOP VIEW



MSOP10

ABSOLUTE MAXIMUM RATING[1)]

VIN, SNS, OUT, PG, GATE, UVLO Pins ..... -0.3V to 100V
OVLO Pin..... -0.3V to 7V
VIN Pin to SNS Pin..... -0.3V to 0.3V
All Other Pins..... -0.3V to 7V
Junction Temperature[2)]…..150ºC
Lead Temperature…….260ºC
Storage Temperature…..... -65ºC to +150ºC
ESD Susceptibility (Human Body Model) .....±2kV
ESD Susceptibility (Charged Device Model) .....±750V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN .....9V to 80V
PG Off Voltage .....0V to 80 V
Operating Junction Temperature .....-40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
MSOP10	156	51ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDTIONS.

2) The JW7221 and JW7221L include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, T_J = -40ºC~125ºC, unless otherwise stated.						
Item	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Units**
INPUT (VIN PIN)						
Input current while enable	I_{IN_EN}	UVLO>2.5V and OVLO<2.5V		0.51	1	mA
Input current while disable	I_{IN_DIS}	UVLO<2.5V or OVLO>2.5V		480	750	μA
Power-on reset threshold at VIN to trigger insertion timer	POR_{IT}	VIN increasing		7.6	8	V
Power-on reset threshold at VIN to enable all functions	POR_{EN}	VIN increasing		8.4	9	V
POR_{EN} hysteresis	POR_{EN_HYS}	VIN decreasing		100		mV
OUTPUT (OUTPIN)						
Output bias current , enable	I_{OUT_EN}	OUT = VIN, Normal operation		1.35		μA
Output bias current , disable	I_{OUT_DIS}	Disabled, OUT =0V, SNS=VIN			20	μA
UVLO, OVLO PINS						
UVLO threshold	$UVLO_{TH}$		2.45	2.5	2.55	V
UVLO hysteresis current	$UVLO_{HYS}$	UVLO = 1 V	12	21	30	μA
UVLO delay	$UVLO_{DLY}$	UVLO high delay to GATE high		55		μs
		UVLO low delay to GATE low		11		
UVLO bias current	$UVLO_{BIAS}$	UVLO = 48 V			1	μA
OVLO threshold	$OVLO_{TH}$		2.4	2.5	2.6	V
OVLO hysteresis current	$OVLO_{HYS}$	OVLO = 2.6 V	12	21	30	μA
OVLO delay	$OVLO_{DLY}$	OVLO low delay to GATE high		55		μs
		OVLO high delay to GATE low		11		
OVLO bias current	$OVLO_{BIAS}$	OVLO = 2.4V			1	μA
POWER LIMIT						
Power limit sense voltage (VIN-SNS)	PWR_{LIM_1}	SNS-OUT = 48V, R_{PWR}=150kΩ	19	25	31	mV
	PWR_{LIM_2}	SNS-OUT = 24V, R_{PWR} =75kΩ	19	25	31	mV
PWR pin current	I_{PWR}	V_{PWR} =2.5V		20		μA
GATE CONTROL						
Gate source current	I_{GATE}	Normal operation, GATE-OUT =5V	14	19	24	μA
Gate sink current		UVLO < 2.5 V	1.75	2	2.6	mA
		VIN to SNS = 150mV or VIN < POR_{IT}, V_{GATE} = 5 V	140	200	260	mA
Gate output voltage in normal operation	V_{GATE}	GATE-OUT voltage	11	12	13	V
CURRENT LIMIT						

Current limit threshold voltage	V_{CL}	VIN-SNS voltage	48.5	55	61.5	mV
CIRCUIT BREAKER						
Circuit breaker threshold voltage	V_{CL}	VIN-SNS voltage	80	105	130	mV
Circuit breaker response time	t_{CB}	VIN-SNS stepped from 0 mV to 80 mV		0.44	1.2	μs
TIMER (TIMER PIN)						
TIMER upper threshold	V_{TMRH}		3.7	3.93	4.16	V
TIMER lower threshold	V_{TMRL}	Restart cycles (JW7221)	1.15	1.23	1.31	V
		End of 8th cycle (JW7221)		0.3		V
		Re-enable Threshold (JW7221L)		0.3		V
Insertion time current	I_{TMR}		3	5.5	8	μA
Sink current , end of insertion time		TIMER pin = 2 V	1	1.5	2	mA
Fault detection current			51	85	120	μA
Fault sink current			1.25	2.5	3.75	μA
Fault restart duty cycle[5)]	DC_{Fault}			0.5%		
POWER GOOD (PGPIN)						
Power good threshold measured at SNS-OUT	PG_{TH}	Decreasing	0.67	1.25	1.85	V
		Increasing, relative to decreasing threshold	0.95	1.25	1.55	
PG output low voltage	PG_{VOL}	I_{SINK} = 2 mA		60	150	mV
PG off leakage current	PG_{IOH}	V_{PG} = 80 V			1	μA

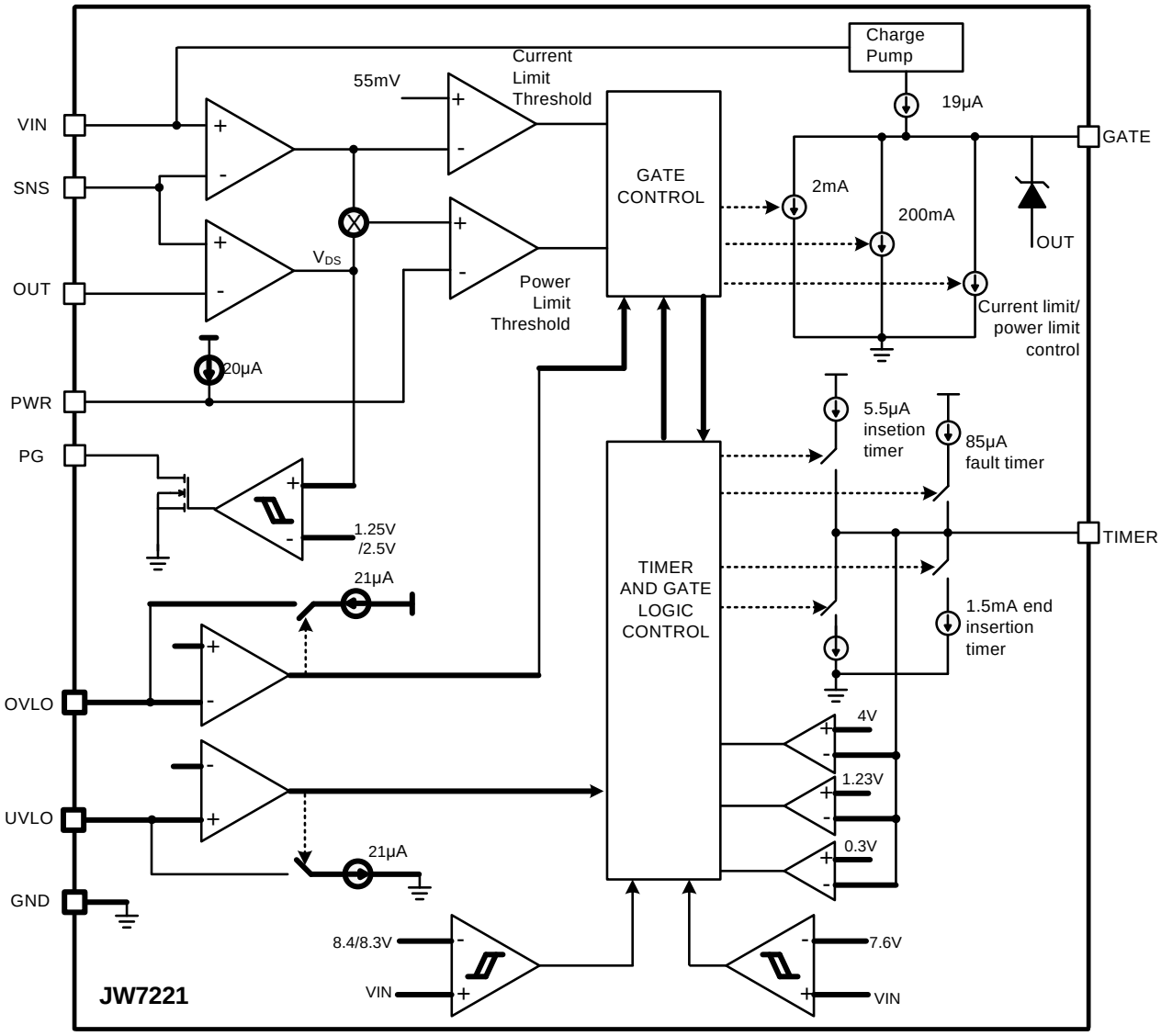
Note:

5) Guaranteed by design.

PIN DESCRIPTION

Pin MSOP10	Name	Description
1	SNS	Current sense input. Used to measure current and regulate it. Kelvin sense is necessary to ensure accurate current limits
2	VIN	Input sense and power supply
3	UVLO	Under-voltage lockout. Under voltage protection threshold and hysteresis can be programmed via external resistor divider.
4	OVLO	Over-voltage lockout. Over voltage protection threshold and hysteresis can be programmed via external resistor divider.
5	GND	Ground.
6	TIMER	Timing set pin. The fault timeout period is programmed by an external capacitor connected from this pin to GND.
7	PWR	Power limit set. The maximum power dissipation for the external MOSFET can be set by an external resistor connected from this pin to GND.
8	PG	Active high. An open drain power good indicator.
9	OUT	Output feedback. Used to measure the voltage across the MOSFET for power limit protection.
10	GATE	Gate driver output for external MOSFET

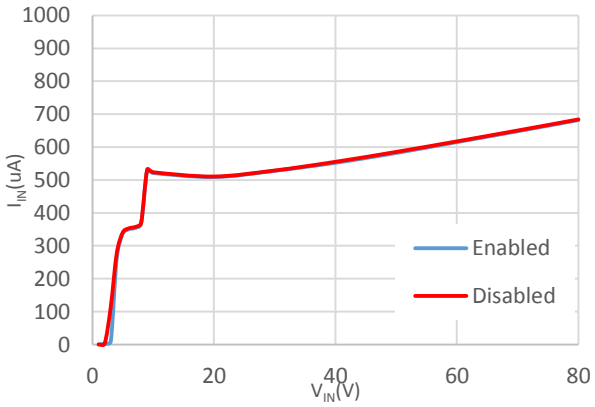
BLOCK DIAGRAM



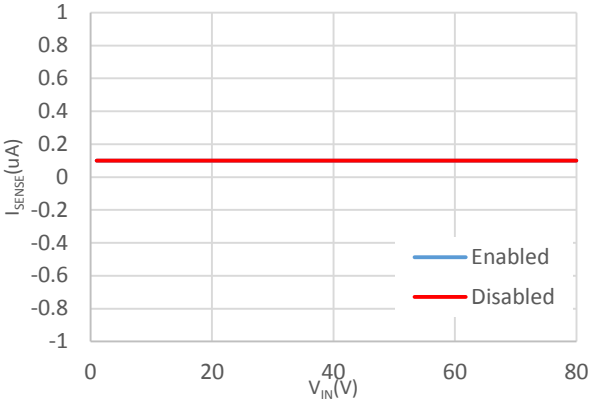
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, T_A = +25°C, unless otherwise noted

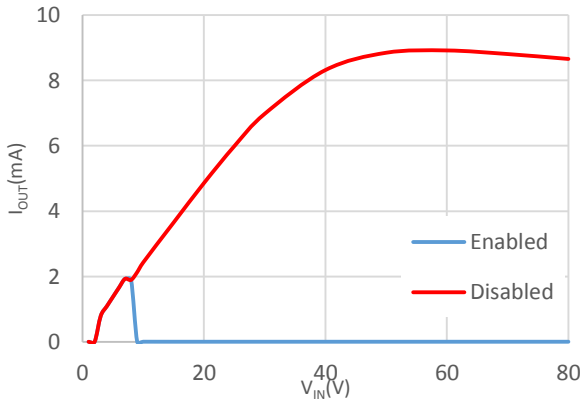
V_{IN} Input Current Vs. Input Voltage



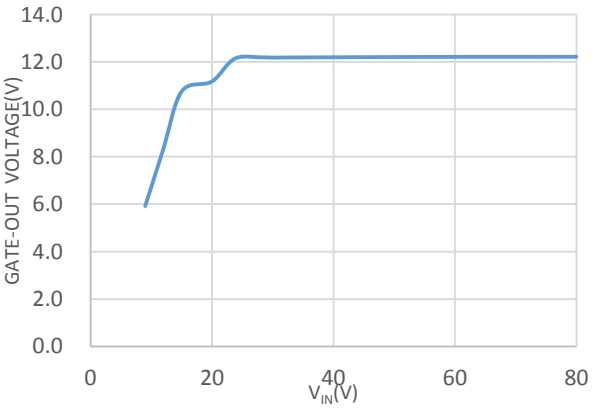
SENSE Pin Input Current Vs. Input Voltage



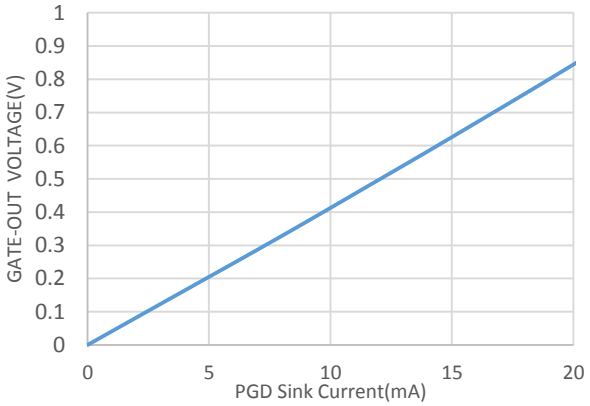
Out Pin Current VS. Input Voltage



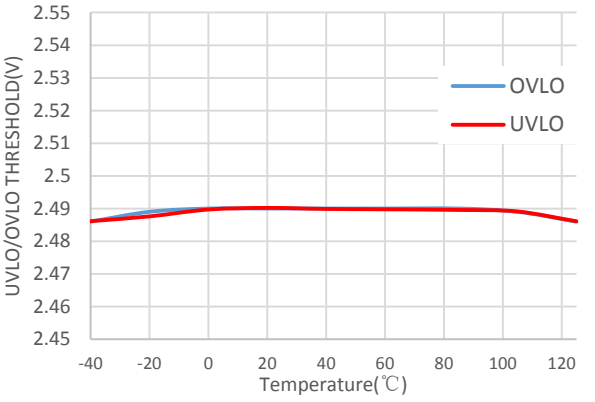
GATE Voltage VS. Input Voltage



PGD Pin Low Voltage VS. Sink Current



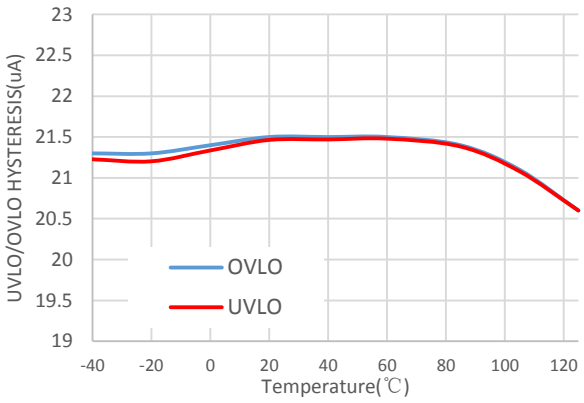
OVLO/UVLO Threshold VS. Temperature



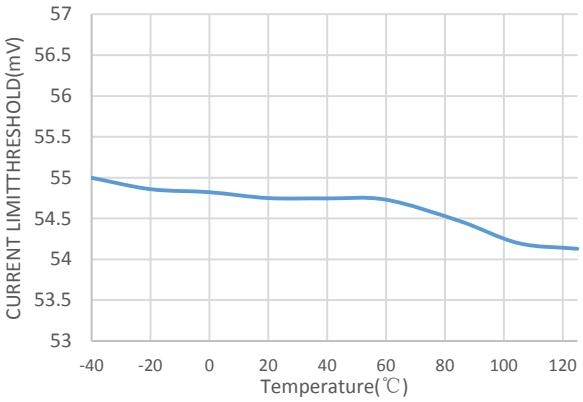
TYPICAL PERFORMANCE CHARACTERISTICS*(continued)*

V_{IN} = 48V, T_A = +25°C, unless otherwise noted

OVLO/UVLO Hysteresis Vs. Temperature



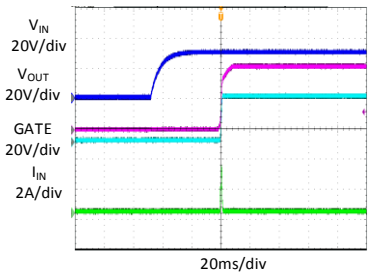
Current Limit Threshold Vs. Temperature



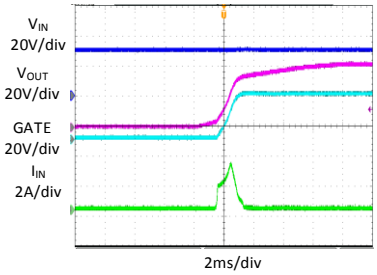
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 30V, T_A = +25°C, unless otherwise noted

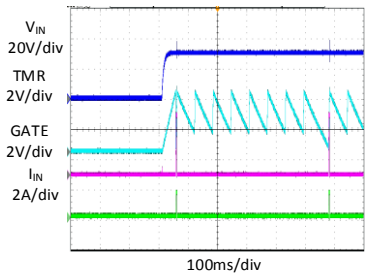
Startup
V_{IN}=30V, P_{LIM}=40W, ILIM=10A



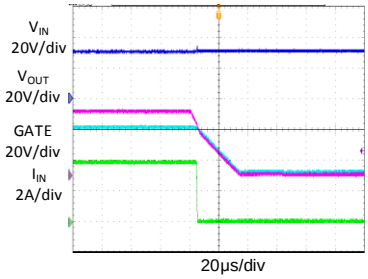
Startup Zoomed In
V_{IN}=30V, P_{LIM}=40W, ILIM=10A



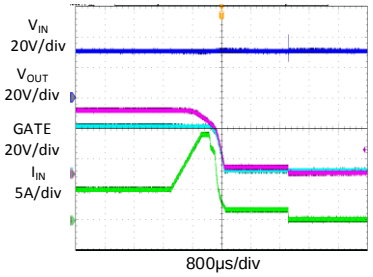
Start Into Short Circuit
V_{IN}=30V, P_{LIM}=40W, ILIM=10A



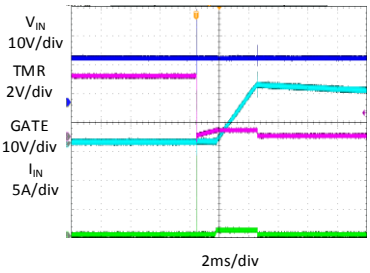
Gradual Over Current
V_{IN}=30V, P_{LIM}=40W, ILIM=10A



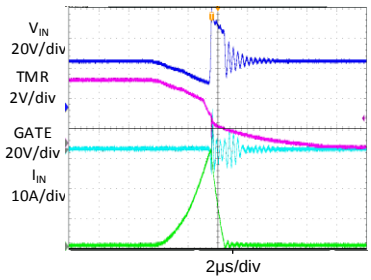
Load Step
V_{IN}=30V LOAD=5A->14A



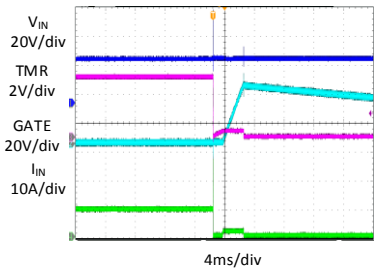
Hot Short
V_{IN}=30V Load=0A, P_{LIM}=40W, ILIM=10A



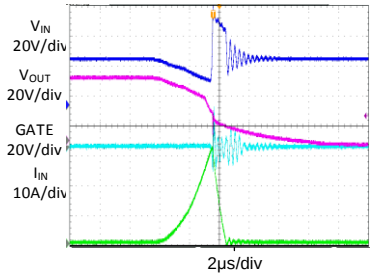
Hot Short Zoomed In
V_{IN}=30V Load=0A, P_{LIM}=40W, ILIM=10A



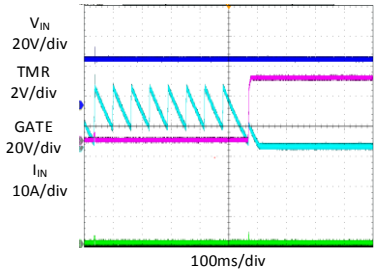
Hot Short
V_{IN}=30V Load=9A, P_{LIM}=40W, ILIM=10A



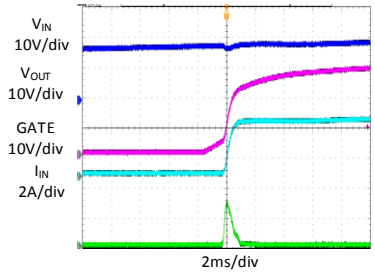
Hot Short Zoomed In
V_{IN}=30V Load=9A, P_{LIM}=40W, ILIM=10A



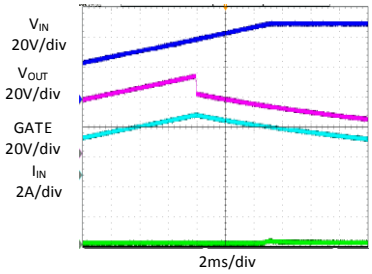
Short Circuit Protection
V_{IN}=30V, P_{LIM}=40W, ILIM=10A



Under Voltage Protection
V_{IN}=0V->30V, UV=15V



Over Voltage Protection
V_{IN}=20V->50V, OV=39V



FUNCTIONAL DESCRIPTION

The JW7221 and JW7221L are hot swap controllers that provide inrush current limit protection thereby allowing a board to be safely inserted and removed from a live backplane. Current limit and power limit protection prevent system against hot short circuit or power supply transient events.

Power Up Sequence

As initially increases, the gate of external N-channel MOSFET is pull down by 200mA current. The 200mA pull down current prevents an inadvertent turn-on as the Miller capacitor of external MOSFET is charged. Additionally, the TIMER pin is initially pull down to GND until VIN reaching POR_{IT} threshold. During the insertion time (t_1), the gate of external MOSFET is held off by 2mA sinking current and TIMER pin is charged by 5.5uA sourcing current. The insertion time prevent MOSFET turn-on while VIN ringing and transients. The insertion time will continue until the voltage of TIMER reaching 4V then C_{TMR} is pull down by 1.5mA sinking current. The duration of insertion time can be computed using equation below:

$$t_{insertion\_time} = \frac{C_{TMR} \times 4V}{5.5\mu A}$$

After the insertion time, the JW7221 control circuitry is enabled when VIN reaches the POR_{EN} threshold. The GATE pin is turned on when the voltage of UVLO exceeds the UVLO threshold (2.5V) and the inrush time (t_2) is beginning.

The GATE of external MOSFET is charged by 19μA souring current and the maximum V_{GS} voltage is clamped below 12V by internal circuit. During the inrush time, the inrush current is limited by current limit or power limit protection. An internal 85μA sourcing current charges C_{TMR} while current limit or power limit protection is active. If the power dissipation and current of MOSFET reduce below limiting threshold before the voltage of TIMER reaching 4V, the inrush time ends and 85μA sourcing current is switched off, then C_{TMR} is discharged by 2.5μA sinking current. If the current limit and power limit protection is still active when the voltage of C_{TMR} reaches 4V. A fault condition is declared and the external MOSFET is turned off. JW7221 enters into retry mode while JW7221L latches off. To avoid timeout during inrush time, C_{TMR} can be computed by below equation:

$$C_{TMR} \geq \frac{t_{inrush\_time} \times 85\mu A}{4V}$$

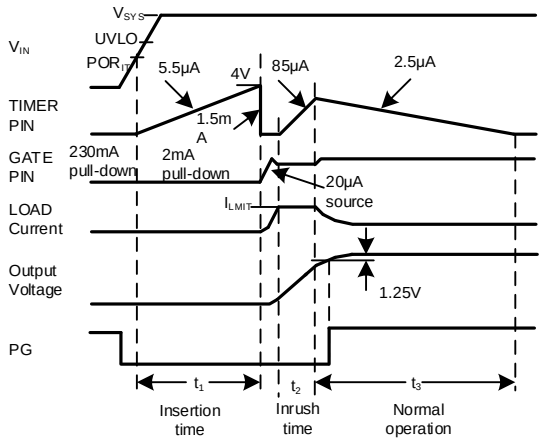


Figure 1. Power-Up Sequence (Current Limit Only)

GATE Control

A charge pump sources 19μA to enhance the external MOSFET. The voltage between GATE to source is limited by internal clamp circuit. The gate of external MOSFET is held charged by 19μA sourcing current to approximately 12V above OUT during normal operation time (t_3). An external Zener diode is recommended if the maximum VGS rating of the external MOSFET is less than 12V. The forward current rating of the external Zener diode should be larger than

250mA.

When the system voltage is initially applied, the GATE pin is held low by a 200mA pull-down current. This helps prevent an inadvertent turn-on as the Miller capacitor of the external MOSFET is charged.

During the insertion time (t_1) the GATE is keeping pull down by 2mA sinking current. The external MOSFET is hold off until the end of t_1. During the inrush time (t_2), the GATE voltage is modulated to regulate the current or power dissipation level.

If the current limit and power limit protection is still active when the voltage of C_{TMR} reaches 4V. The GATE is pull down by 2mA current. A fault condition is declared. If the power dissipation and current of MOSFET reduce below limiting threshold before the voltage of TIMER reaching 4V, The GATE is held charging and JW7221/JW7221L enters normal operating time.

If under voltage protection or over voltage protection is triggered, the GATE pin is pulled low by the 2mA pull-down current to turn off the external MOSFET.

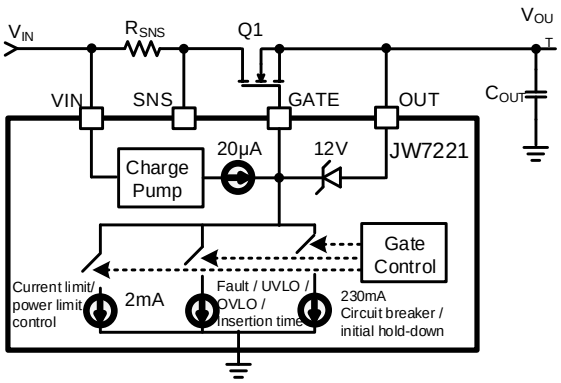


Figure 2. GATE Control

Fault Timer and Restart

If the current limit or power limit protection is still active when the voltage of TIMER reaches 4V, the GATE is held off by 2mA current. Then the JW7221L latches off so that GATE pin is pull down by 2mA current and C_{TMR} is discharged by 2.5µA current. Latch off mode is continue until JW7221L is reset by VCC, UVLO or OVLO.

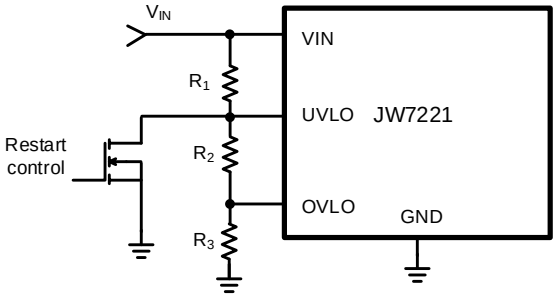


Figure 3. Latched Fault Restart Control

The JW7221 enters automatic restart sequence. The TIMER pin continues to charge and discharge between 1.23V and 4V seven times as shown in Figure 4. During restart sequence, the C_{TMR} charging current is 85µA while discharging current is 2.5µA. When the TIMER pin reaches 0.3V during the eighth high to low ramp, the 19µA current sourcing at the GATE pin turns on external MOSFET. If the fault condition is not removed, the timeout period and the restart cycle repeat.

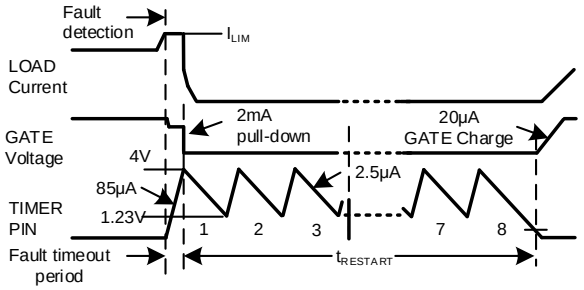


Figure 4. Restart Sequence

Shutdown Control

The external MOSFET can be remotely turned off by pull UVLO pin low or pull OVLO pin high. Both UVLO and OVLO threshold is 2.5V. Typical application is shown as Figure 5.

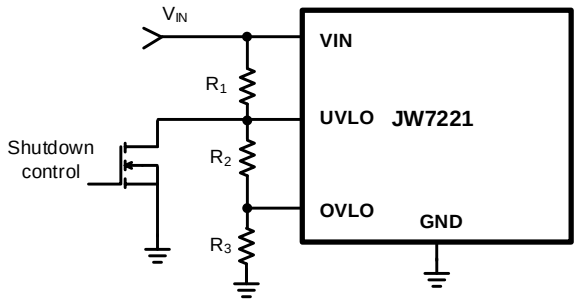


Figure 5. Shutdown Control

Current Limit

The load current is measured by the voltage between VIN and SNS. The current limit protection is active when the voltage across the sense resistor R_{SNS} reaches 55mV. In the current limit condition, the GATE is modulated to regulate the voltage across R_{SNS} around 55mV and C_{TMR} is charged by internal 85μA sourcing current. If the load current decrease below 55mV before the voltage of TIMER reaching 4V, IC recover to normal operation mode. The R_{SNS} resistor is recommended to be smaller than 100 mΩ.

Circuit Breaker

The JW7221 and JW7221L incorporates two distinct thresholds: a current limit threshold (55mV) and a fast-trip threshold. The fast-trip threshold protect the system against a serve over load and hot short circuit. When the voltage across the sense resistor R_{SNS} exceeds the 105mV fast trip threshold, the GATE pin immediately pulls the external MOSFET gate to ground with approximate 200mA, and a fault time-out period begins. When the voltage across R_{SNS} falls below 105 mV, the 200mA pull-down current at the GATE pin is switched off, and the gate voltage of external MOSFET is then modulated to regulate load current.

Power Limit

The power limit protection allows the better utilization of external MOSFET's SOA. In most cases, inrush current is limited by power limit function. The power dissipation is calculated by multiplying the V_{DS} (V_{SNS}-V_{OUT}) of the external MOSFET and the voltage across R_{SNS}. The power limit is programmed by the external resistor connected between PWR and GND. When the power limit is active, the GATE is modulated to regulate the power dissipation around power limit threshold. The power limit program resistor (R_{PWR}) can be calculated using following equation:

$$R_{PWR} = 1.3 \times 10^5 \times R_{SNS} \times P_{LIM}$$

The power limit program resistor is recommended to be smaller than 150kΩ.

Under-voltage Lockout (UVLO)

Both threshold and hysteresis can be programmed for under voltage protection. The UVLO rising threshold is set by R_1 and R_2 (shown in Figure 6) according to below equation:

$$UVLO_{rising} = \frac{R_1 + R_2}{R_2} \times 2.5V + R_1 \times 21\mu A$$

The hysteresis of UVLO is shown below:

$$UVLO_{hyst} = R_1 \times 21\mu A$$

The UVLO pin sinks 21μA current when VIN is below $UVLO_{rising}$. When VIN rise up above $UVLO_{rising}$, the 21μA sinking current is switched off and GATE is pull up by 19μA if the insertion time is finished. In general, the rising UVLO threshold should be sufficiently below the minimum input voltage.

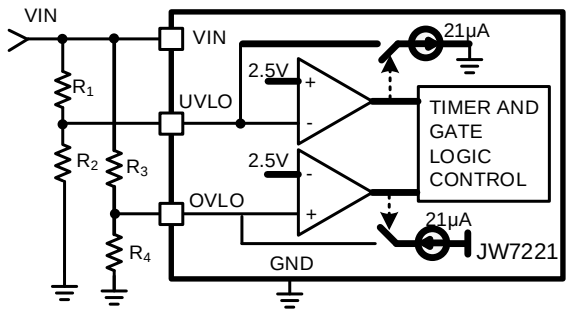


Figure 6. UVLO and OVLO Thresholds Set By R1-R3

Over-voltage Lockout (OVLO)

Both threshold and hysteresis can be programmed for over voltage protection. The OVLO rising threshold is set by R3 and R4 (shown in Figure 6) according to below equation:

$$OVLO_{falling} = \frac{R_3 + R_4}{R_4} \times 2.5V - R_3 \times 21\mu A$$

The hysteresis of OVLO is shown below:

$$OVLO_{hyst} = R_3 \times 21\mu A$$

The OVLO pin sources 21μA current when VIN is above $OVLO_{rising}$. When VIN falling down below $OVLO_{falling}$, the 21μA sourcing current is switched off and GATE is pull up by 19μA if the insertion time is finished. In general, the falling OVLO threshold should be sufficiently above the maximum input voltage.

Power Good Indicator

The Power Good pin is an open drain indicator. Before insertion time, when VIN increases above 5V PG switches low. PG keeps low until the voltage of OUT pin increases to V_{SNS}-1.25V (V_{DS}<1.25V). The PG pin keeps high until the drain-source voltage of the external MOSFET is above 2.5V. A pull up resistor (R_{PG}) is recommended as shown in Figure7. It's critical to keep the downstream DC/DC off while the hot swap is charging the bulk capacitor. This can be accomplished through the PG pin.

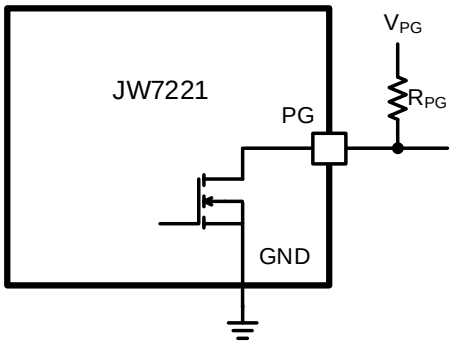


Figure 7. Power Good Output

APPLICATION INFORMATION

The JW7221 and JW7221L are hot swap controller for 12~72V system application and is used to manage inrush current and protect downstream circuitry and upstream bus in case of fault condition.

Typical Application

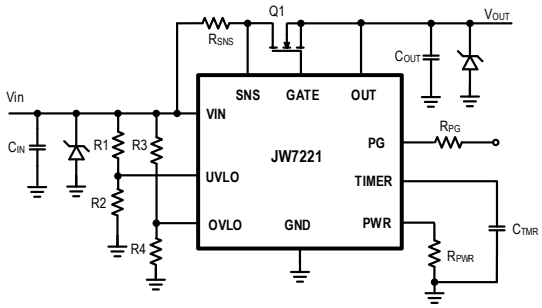


Figure 8. Typical Application

Design Requirements

The table below summarizes the design parameters that must be known before designing a hot swap circuit. Keeping load off until hot swap is fully powered up is recommended and it can be realized by using PG function. Starting load early causes unnecessary stress on external MOSFET and could lead to MOSFET failure to startup.

PARAMETER	VALUE
Input Voltage Range	18~36V
Maximum Load Current	7A
UVLO Falling Threshold	14V
UVLO Hysteresis	2V
OVLO Rising Threshold	38V
OVLO Hysteresis	2V
C_{OUT}	100μF
Maximum Ambient Temperature	50ºC

R_{SNS} Selection

Before selecting R_{SNS}. First compute the maximum load current I_{max}. To provide some margin, set the target current I_{CL} to 1.5×Imax and compute R_{SNS} using equation below:

$$R_{SNS} = \frac{55mV}{1.5 \times I_{max}} = \frac{55mV}{1.5 \times 7A} = 5.23m\Omega$$

Using next available R_{SNS} of 5mΩ. Current limit can be computed as 11A. In addition, if a precise current limit is desired, a sense resistor with a resistor divider can be used as shown in Figure 9.

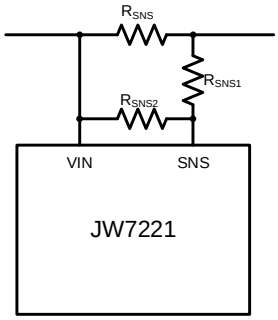


Figure 9. SENSE Resistor Divider

The current limit using resistor divider can be calculated as below equation:

$$i_{CL} = \frac{55mV}{R_{SNS}\frac{R_{SNS2}}{R_{SNS1} + R_{SNS2}}}$$

The R_{SNS1} is recommended to be smaller than 10Ω.

External MOSFET Selection

The JW7221/JW7221L drives external N-channel MOSFETs to limit inrush current and protect system from fault condition such as over current, over voltage and under voltage. The important features of the MOSFETs are $R_{DS(ON)}$, the maximum drain-source voltage and the SOA. Device with V_{GS} lower than 12V rating can be used if a Zener diode is connected. Sufficient $V_{DS(MAX)}$ margin is recommended because the MOSFET may experience much higher

transient voltages during extreme conditions. A MOSFET with a $V_{DS(MAX)}$ rating of at least twice the maximum input supply voltage is recommended.

The next factor need to consider is $R_{DS(ON)}$, The maximum voltage droop across MOSFET should be less than power good threshold 140mV.

$$R_{DS(ON)} \leq \frac{140mV}{11A} = 12.7m\Omega$$

Taking these factors into consideration, the IPBO27N10N5 is selected for this example. The MOSFET has a maximum gate-source rating of 20V. and maximum $R_{DS(ON)}$ of 2.7mΩ. The $R_{\theta JC}$ is 0.6 ºC/W while $R_{\theta JA}$ is 62 ºC/W.

The effect of R_{DSON} upon the maximum operating temperature should be considered by following equation.

$$R_{DS(ON)} \leq \frac{T_{J\_MAX} - T_{A\_MAX}}{{I_{MAX}}^2 \times R_{\theta JA}} = \frac{130 - 50}{11^2 \times 62} = 10.6m\Omega$$

Power Limit Selection

In general, the power limit P_{LIM} of the JW7221/JW7221L should be set to prevent the die temperature from exceeding a short-term maximum temperature T_{JMAX} of the MOSFET. Usually T_{JMAX} of the MOSFET could be set as 130. Leave some margin to usual manufacture's rating 150ºC. P_{LIM} can be set by following equation:

$$P_{LIM} \leq \frac{T_{J\_MAX} - ({I_{MAX}}^2 \times R_{DS(ON)} \times R_{\theta CA} + T_{A\_MAX})}{R_{\theta JC}} = \frac{130 - (11^2 \times 0.0027 \times 62 + 50)}{0.6} = 130W$$

$V_{SNS\_PL\_MIN}$ is the minimum sense voltage during power limit operation. Usually $V_{SNS\_PL\_MIN}$ is measured when drain-source voltage is max. Due to offsets of internal amplifiers, programmed power limit (P_{LIM}) accuracy degrades at low $V_{SNS\_PL\_MIN}$ and could cause start-up issues. To ensure reliable operation, verify that $V_{SNS\_PL\_MIN}$>5mV using below equation

$$V_{SNS\_PL\_MIN} = \frac{P_{LIM} \times R_{SNS}}{V_{IN\_MAX}}$$

Therefore, the P_{LIM} should be larger than 36W. Take this factors into consideration, P_{LIM} is set as 40W. The maximum power dissipation of the external MOSFET can be programmed by an external resistor R_{PWR}. The value of R_{PWR} can be computed by following equation.

$$R_{PWR} = 1.3 \times 10^5 \times R_{SNS} \times P_{LIM}$$

R_{PWR} can be computed as 26kΩ for this example. The next available value is 25kΩ.

C_{TMR} Selection

The fault timeout time should be larger than the maximum output voltage rise time. It is critical to keep downstream DC/DC converter off while the hot swap is charging bulk capacitor. If the P_{LIM}<I_{LIM}×V_{IN_MAX}, the estimated startup time can be computed by following equation:

$$t_{start} = \frac{C_{OUT}}{2} \times \left(\frac{{V_{IN\_MAX}}^2}{P_{LIM}} + \frac{P_{LIM}}{{I_{LIM}}^2} \right)$$

If the P_{LIM}>I_{LIM}×V_{IN_MAX}, the startup time can be calculated by below equation:

$$t_{start} = \frac{C_{OUT} \times V_{IN\_MAX}}{I_{LIM}}$$

For this application, P_{LIM}<I_{LIM}×V_{IN_MAX}, the t_{start} can be estimated as 1.63ms. To ensure that fault timeout cannot be triggered during inrush time, 50% fault timeout margin is recommended. C_{TMR} can be computed with following equation.

$$C_{TMR} = \frac{t_{FLT} \times 85\mu A}{4V} = \frac{150\% \times 1.94ms \times 85\mu A}{4V}$$

The next available C_{TMR} is chosen as 68nF. The

t_{FLT} can be calculated by below equation:

$$t_{FLT} = \frac{C_{TMR} \times 4V}{85\mu A} = \frac{68nF \times 4V}{85\mu A} = 3.2ms$$

SOA Check

Once the power limit and fault timer are chosen, it's critical to check the MOSFET's SOA during all conditions. In the worst case. The MOSFET's VDS equals the maximum input supply voltage, and maximum current equal to P_{LIM}/V_{IN_MAX}, the stress event lasts for t_{FLT}.

For this application, IPBO27N10N5 need to survive during 36V 1.11A for 3.2ms. Based on the SOA of IPBO27N10N5, it can handle 40V 1.05A for 10ms and 40V 4A for 1ms. The SOA for 3.2ms can be extrapolated by approximating SOA versus time as a power function as shown below

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln\frac{I_{SOA}(t_1)}{I_{SOA}(t_2)}}{\ln\frac{t_1}{t_2}} = \frac{\ln(\frac{4A}{1.05A})}{\ln(\frac{1ms}{10ms})} = -0.58$$

$$a = \frac{I_{SOA}(t_1)}{{t_1}^m} = \frac{4A}{(1ms)^{-0.58}}$$

$$I_{SOA}(3.2ms) = 4A \times (1ms)^{0.58} \times 3.2^{-0.58} = 20.03A$$

Note that the SOA of a MOSFET is specified at a case 25 ºC. While the case temperature can be much hotter during a hot-short. The SOA must be derated based on T_{C_MAX} using equation following:

$$T_{C\_MAX} = T_{A\_MAX} + R_{\theta CA} \times {I_{MAX}}^2 \times R_{DS(ON)}$$

$$= 50 + 61.4℃/W \times 11A^2 \times 2.7m\Omega = 70℃$$

$$I_{SOA}(3.2ms, T_{C\_MAX})$$

$$= I_{SOA}(3.2ms, 25℃)\frac{T_{J\_MAX} - T_{C\_MAX}}{T_{J\_MAX} - 25℃}$$

$$= 2.03A \times \frac{175 - 70}{175 - 25} = 1.42A$$

Based on calculation the MOSFET can handle 1.42A, 36V for 3.2ms. This means the MOSFET is not at risk of getting damaged during a hot-short.

UVLO and OVLO Setting

Both the threshold and hysteresis can be programmed by external resistor divider. Usually the rising UVLO threshold should be set sufficiently below the minimum input voltage and the falling OVLO threshold should be set sufficiently above the maximum input voltage. For this example, UV rising threshold is 16V and UV falling threshold is 14V. R_1 can be chosen according to 2V UV threshold.

$$R_1 = \frac{UV_{hyst}}{21\mu A} = \frac{2V}{21\mu A} = 95k\Omega$$

R_2 can be computed by equation shown as

$$R_2 = \frac{R1}{UV_{falling} - 2.5V} = \frac{95k\Omega}{14 - 2.5} \times 2.5 = 20.6k\Omega$$

The OV setting can be programmed as a similar fashion as shown in equations below

$$R_3 = \frac{OV_{hyst}}{21\mu A} = \frac{2V}{21\mu A} = 95k\Omega$$

$$R_4 = \frac{R_3}{OV_{rising} - 2.5V} = \frac{95k\Omega}{38 - 2.5} \times 2.5 = 6.69k\Omega$$

Choose available value as R_1=R_3=100kΩ, R_2=20kΩ, R_4=6.8kΩ.

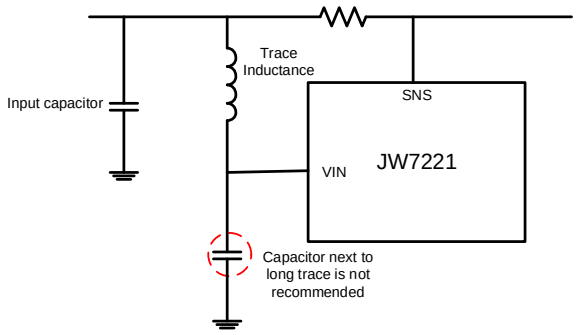
Final Schematic and Component Values

PARAMETER	VALUE
R_{SNS}	5mΩ
R_1	100kΩ
R_2	20kΩ
R_3	100kΩ
R_4	6.8kΩ
R_{PWR}	25kΩ
Q_1	IPBO27N10N5
C_{TMR}	68nF
C_{OUT}	100μF

PCB Layout Note

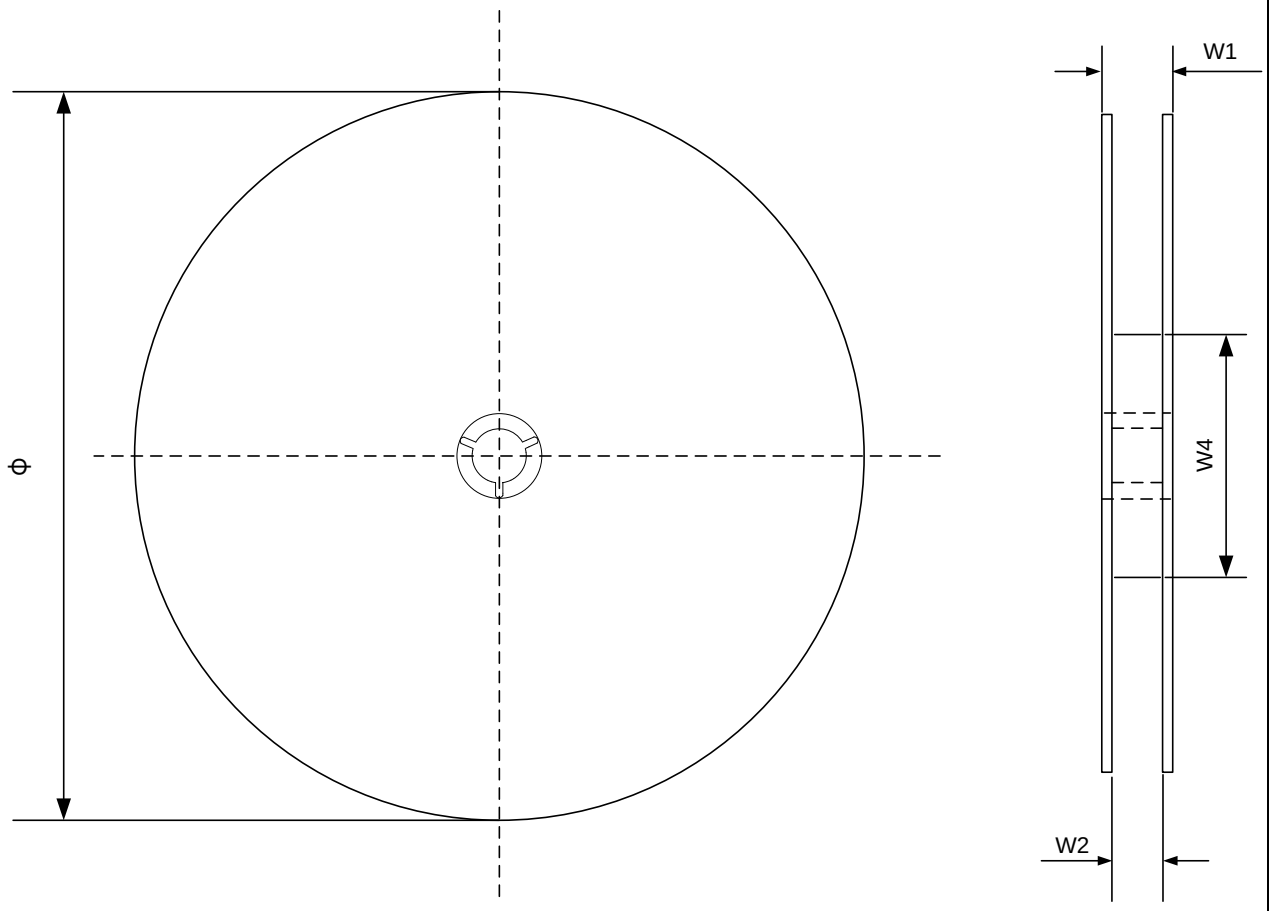
For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. VIN pin and SNS pin need to have a Kelvin Sense connection to the sense resistor R_{SNS}.
2. A Shottky diode is recommended to be connected From GND to OUT pin.
3. A large voltage can develop between VIN and SNS, if the bypass capacitor is placed right next to the pin and the trace from RSNS to the pin is long, a LC filter is formed. This could result in a violation of the ABS max rating from VCC to SNS.
4. Keep the input capacitor on VIN pin as close to the IC as possible.



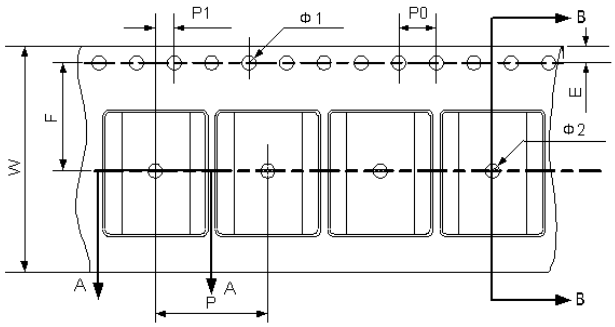
TAPE AND REEL INFORMATION

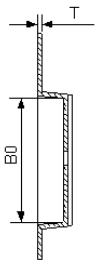
Reel UNIT: mm



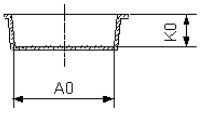
Package	Diameter Φ	Thickness W1	Width W2	W4
MSOP10	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm





SECTION B-B

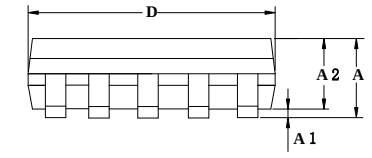


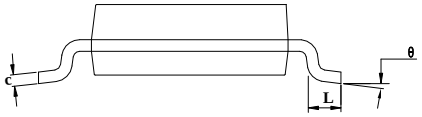
SECTION A-A

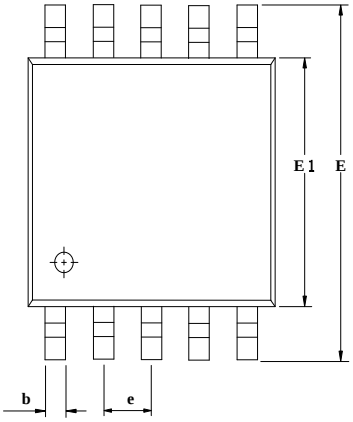
Package	P0	P1	P	A0	B0	W	T0	K0	Φ1	Φ2	E	F
MSOP10	4.0±0.1	2.0±0.05	8.0±0.1	5.2±0.1	3.3±0.1	12 +0.30 −0.10	0.25±0.02	1.2min	1.5 +0.10 −0.00	1.5 +0.25 −0.00	1.75±0.1	5.50±0.05

PACKAGE OUTLINE

MSOP10 UNIT: mm

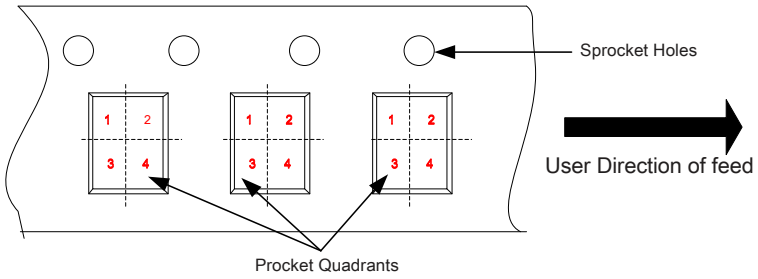






Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.02	—	0.15
A2	0.75	—	0.95
b	0.18	—	0.33
c	0.09	—	0.23
D	2.90	3.00	3.10
E	4.75	—	5.05
E1	2.90	—	3.10
e	0.50(BSC)		
L	0.40	—	0.80
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package	Pin1 Quadrant
MSOP10	1

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