JW7202

Dual Channel Low Side ORing Controller and Monitor

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®7202 is a low side ORing FET controller, which can operate in conjunction with two external MOSFETS as ideal diodes rectifier when connected in series with power sources. Besides, the power consumption, heat dissipation and PC board area also can be reduced by using the diode-OR with N-channel MOSFETS instead of Schottky diodes.

In the forward direction the JW7202 controls the voltage drop across the MOSFETs to ensure smooth current transfer from one path to the other without oscillation. If a power source fails or is shorted, fast turnoff minimizes reverse current transients.

JW7202 offers SOP8 package.

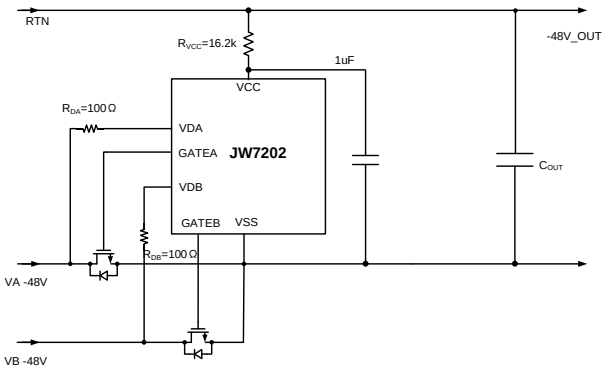
FEATURES

- Replaces Power Schottky Diode
- Controls N-Channel MOSFETs
- 200V Absolute Maximum
- 0.3μs Turn-Off Time Limits Peak Fault Current
- Smooth Switchover without Oscillation
- No Reverse DC Current
- Regulation: 25 mV ±15 mV
- Fast Turn off: –25 mV ±15 mV
- Available in 8-Lead SOP Package

APPLICATIONS

- High Availability Systems
- Advanced TCA® (ATCA) Systems
- ±48V Distributed Power Systems
- Computer Systems/Servers
- Telecom Infrastructure
- Optical Networks

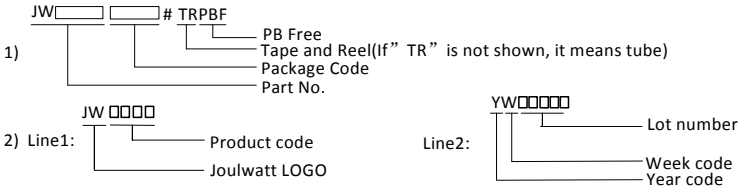
TYPICAL APPLICATION



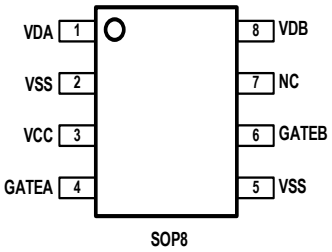
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW7202SOPB#TRPBF	SOP8	JW7202 YW□□□□□

Note：



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1) 2)]

Supply Voltage----V_{CC} (current into V_{CC} <10 mA)..... -0.3V to 20V
Input Voltage----V_{DA}, V_{DB}..... -0.3V to 200V
Output Voltage----V_{GATEA},V_{GATEB} ..... -0.5V to V_{CC}
Junction Temperature[3)]…….....150ºC
Lead Temperature……..……260 ºC
Storage Temperature……. .....-55ºC to 150ºC

RECOMMENDED OPERATING CONDITIONS[4)]

V_{VCC}----External supply voltage……..... 0V to 10.5V
V_{VCC}----Internal clamp voltage (current into V_{CC} <10 mA))....0V to 14V
V_{DA}, V_{DB}…….....-0.2V to 150V
V_{GATEA}, V_{GATEB}..... 0V to V_{CC}
R_{DA}, R_{DB}.....0 Ω to 2kΩ
Operation Junction Temperature……..…-40~125ºC

THERMAL PERFORMANCE[5)]

	θ_{JA}	θ_{JC}
SOP8….....	116.....	62ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDE OPERATING CONDTIONS.
2) All currents into pins are positive, all voltage are referenced to VSS unless otherwise specified.
3) The JW7202 includes thermal protection that is intended to protect the device in overload condition. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A =-40~125°C, 2 mA < I_{VCC} < 10 mA, –1V < V_D < 150 V; All pin voltages are relative to VSS (unless otherwise noted).

Item	Symbol	Condition	Min.	Typ.	Max.	Units
V_{CC}						
UVLO on V_{CC}	$V_{(UVLO\_VCC)}$	V_{CC} rising		6.4	7	V
UVLO hysteresis on V_{CC}	$V_{(UVLO\_,hyst)}$	hysteresis		0.6		V
V_{CC} internal regulator voltage	$V_{(VCC\_INT)}$	1.1< $I_{(VCC)}$ < 10 mA (current into V_{CC})		11		V
Quiescent current	Quiescent Current	V_{VCC} = 10 V. On			1.4	mA
		V_{VCC} = 7 V, GATEx in regulation			1	
VDA VDB						
Leakage current	$I_{(lkg,Dx)}$	V_{DX} = –50 mV, GATEx ON	-4		4	µA
		V_{DX} = 150 V, GATEx Off			130	
Forward regulation voltage of the ORing controller. V_{FWD} = V_{SS} – V_{Dx}	$V_{(FWD)}$		10	30	50	mV
Forward voltage where a fast pull up is activated.	$V_{(FWD,FST)}$	GATE = 5 V. V_{SS}– V_{Dx} ↑ measure when I_{GATE}= 100 µA	50	80	105	mV
Fast reverse trip voltage.	$V_{(RV)}$		6	20	30	mV
Response time to large reverse current[5)]	$T_{VD,FST,RESP}$	V_{Dx} steps from -40 mV to 15 mV. Measure time for GATE to come down.		300		ns
GATEA, GATEB						
Gate output voltage	$V_{VCC-GATEx}$				0.25	V
Gate sourcing current in regulation	$I_{(GATEx,SRS)}$	V_{SS} – V_D = 50 mV		30		µA
Gate sinking current in regulation	$I_{(GATEx,SINK)}$	V_{SS} – V_D = 0		30		µA
Pull up resistance in fast sourcing mode.	$R_{GATEx,SRC,FST}$	V_{SS} – V_D = 100 mV; Measure current at V_{GATEx} = 0 V. R = V_{VCC}/I		17		kΩ
Fast Gate pull down current	$I_{(GATEx,FST)}$	V_{SS} – V_{Dx} = –15 mV	0.4	1	1.5	A
OTSD (Over Temperature Shut Down)						
Shutdown temperature[6)]	T_{SD}	Temp Rising		155		ºC
Shutdown temperature Hysteresis[6)]	$T_{SD,hyst}$			8		ºC

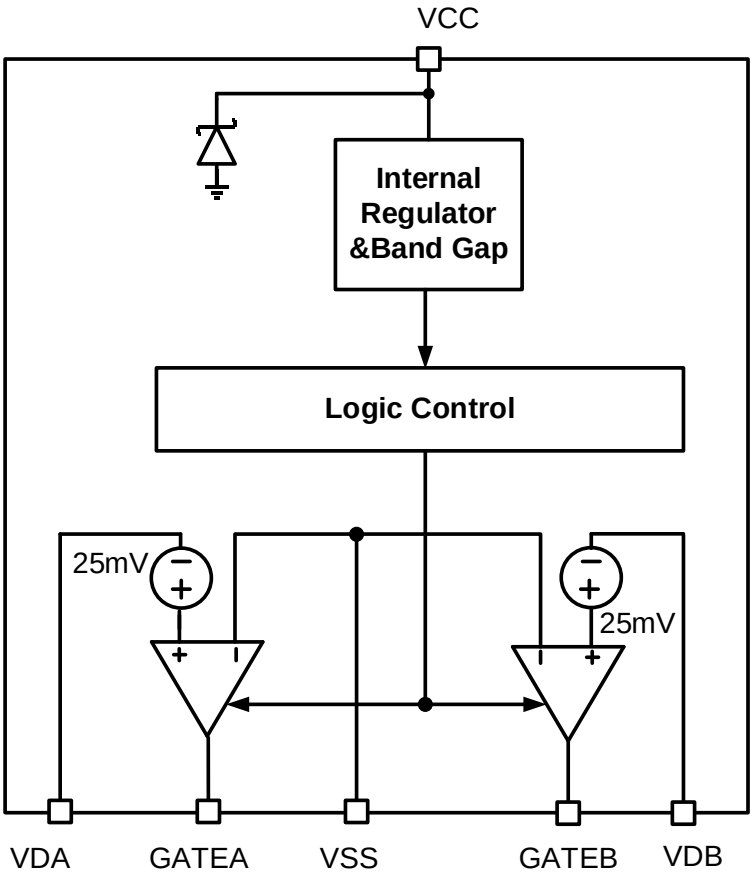
Note：

6) Guaranteed by design.

PIN DESCRIPTION

Name		Description
SOP-8	Pin	
1	VDA	Connected to drain of channel A MOSFET. The JW7202 will regulate the drop from V_{SS} to V_{DA} to 25 mV to mimic an ideal diode.
2	VSS	This pin corresponds to the IC V_{SS}.
3	VCC	Power supply. Tied to external power through a resistor. A 1uF or larger ceramic cap is recommended close to this pin.
4	GATEA	Channel A gate driver for the ORing FET.
5	VSS	This pin corresponds to the IC V_{SS}.
6	GATEB	Channel B gate driver for the ORing FET.
7	NC	Not connected. Leave this pin float or connect this pin to GND.
8	VDB	Connected to drain of channel B MOSFET. The JW7202 will regulate the drop from V_{SS} to V_{DB} to 25 mV to mimic an ideal diode.

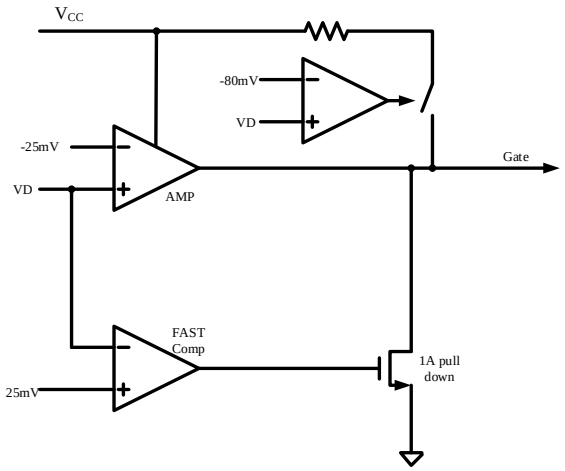
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The JW7202 is an integrated dual channel ORing controller that enables high power telecom systems to comply with stringent transient requirements. ORing diodes have been a popular means of connecting these supplies at the point of load. The disadvantage of this approach is the forward voltage drop and resulting efficiency loss. This drop reduces the available supply voltage and dissipates significant power. Using N-channel MOSFETs to replace Schottky diodes reduces the power dissipation and eliminates the need for costly heat sinks or large thermal layouts in high power applications.

The JW7202 is a low side ideal diode and ORing controller that drives two external N-channel MOSFETs as pass transistor to replace ORing diodes. The V_{SS} and V_{Dx} pins form the anodes and cathodes of the ideal diodes. The source pins of the external MOSFETs are connected to the V_{SS} pin. The drains of the MOSFETs are connected at the V_{Dx} pins. The gates of the external MOSFETs will be driven by the JW7202 to regulate the voltage drop across the pass transistors.



The JW7202 will regulate the forward drop across the ORing FET to 25 mV. This is accomplished by controlling the V_{GS} of the MOSFETs. As the current decreases the V_{GS} is also decreased, which effectively increases the R_{DSON} of the MOSFET. This process is regulated with a low gain amplifier that is gate (ORing FET) pole compensated. The lower gain helps ensure stability over various operating conditions. The regulating amplifier ensures that there is no DC reverse current. However, the amplifier is not very fast and thus it is paired with a fast comparator. This comparator quickly turns off the FET if there is significant reverse current detected.

An internal regulator that can sink up to 10mA clamps the V_{CC} to 11V above V_{SS}. To filter supply transient and supply AC current, A 1uF bypass capacitor is recommended to be connected between V_{CC} and V_{SS}.

APPLICATION INFORMATION

Input Power Supply

The power supply for the device is derived from external power through an external current limiting resistor R_{VCC}. R_{VCC} should be sized in such a way to ensure that sufficient current is supplied to the IC at minimum operating voltage corresponding to the falling under voltage threshold. To ensure Stability of internal loop a minimum of 0.1uF is required for C_{VCC}. A 1uF cap is recommended in typical application. R_{VCC} should be chosen to accommodate the maximum supply current requirement of 2mA at expected input operating voltage, and the supply current should be smaller than 10mA.

$$R_{VCC} \leq \frac{V_{IN\_MIN} - V_{CC\_MAX}}{I_{CC\_MIN}} = \frac{V_{IN\_MIN} - V_{CC\_MAX}}{2mA}$$

$$R_{VCC} \geq \frac{V_{IN\_MAX} - V_{CC\_MIN}}{I_{CC\_MAX}} = \frac{V_{IN\_MAX} - V_{CC\_MIN}}{10mA}$$

The power dissipation of the resistor is calculated at the maximum DC input voltage:

$$P = \frac{(V_{IN\_MAX} - V_{CC\_MIN})^2}{R_{VCC}}$$

If R_{VCC} is shorted, the external supply voltage should be between 7V and 10.5V. Driving V_{CC} beyond 10.5V may damage the part.

MOSFET Failure

Typically, the V_{Dx} pin maximum negative voltage will be defined by the body diode of the external MOSFET. In the event that the external MOSFET has a catastrophic failure that result in an open body diode, the voltage between the V_{Dx} pins and the V_{SS} pin may cause current through the JW7202 substrate diode at the V_{Dx} pins. The voltage at the V_{SS} pin must be limited to a safe level (-1V) to prevent damage to the JW7202. The voltage on the V_{Dx} pins can be limited with the use of a Schottky diode and the current limiting resistor. Note that the power dissipation of the current limiting resistor should allow for any anticipated worst case condition. See Figure1

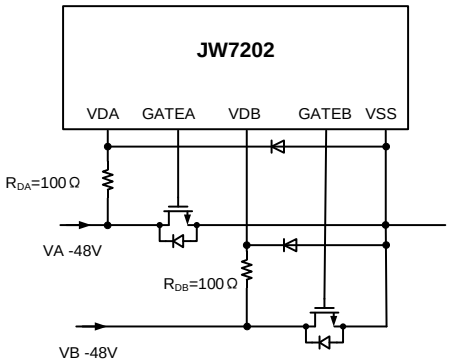


Figure 1. Method of Protecting the DA and DB Pins from Negative Inputs

MOSFET Selection

The JW7202 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are on-resistance R_{DSON}, the maximum drain-source voltage V_{DS}, and the threshold voltage.

The gate drive for the MOSFET is guaranteed to be greater than 10V and less than Vcc. This allows the use of logic level threshold N-channel MOSFET and standard N-channel MOSFET above 10V. An external Zener diode can be used to clamp the potential from the MOSFET's gate to source if the rated breakdown voltage is less than 18V.

The maximum allowable drain-source voltage, BVDSS, must be higher than the supply voltages. If an input is connected to V_{SS}, the full supply voltage will appear across the MOSFETs.

Input Short-Circuit Faults

The dynamic behavior of an active, ideal diode entering reverse bias is most accurately characterized by a delay followed by a period of

reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistances and inductances. During the reverse recovery phase, energy stored in the parasitic inductances is transferred to other elements in the circuit. Current slew rates during reverse recovery may reach 100A/μs or higher.

High slew rates coupled with parasitic inductances in series with the V_{SS} and V_{Dx} paths may cause potentially destructive transients to appear at the V_{Dx} pin of the JW7202 during reverse recovery. A zero impedance short-circuit directly across an input that is supplying current is especially troublesome because it permits the highest possible reverse current to build up during the delay phase.

When the MOSFET is finally switched off, the energy stored in the parasitic wiring inductances will be transferred to the rest of the circuit. As a result JW7202 V_{Dx} pin will see a positive voltage spike. To be robust enough, JW7202 uses high voltage process and can sustain 200V spike voltage. In case of severe condition that the input wire is very long and the positive voltage spike could reach 200V, a Schottky diode shown in Figure2 can be added.

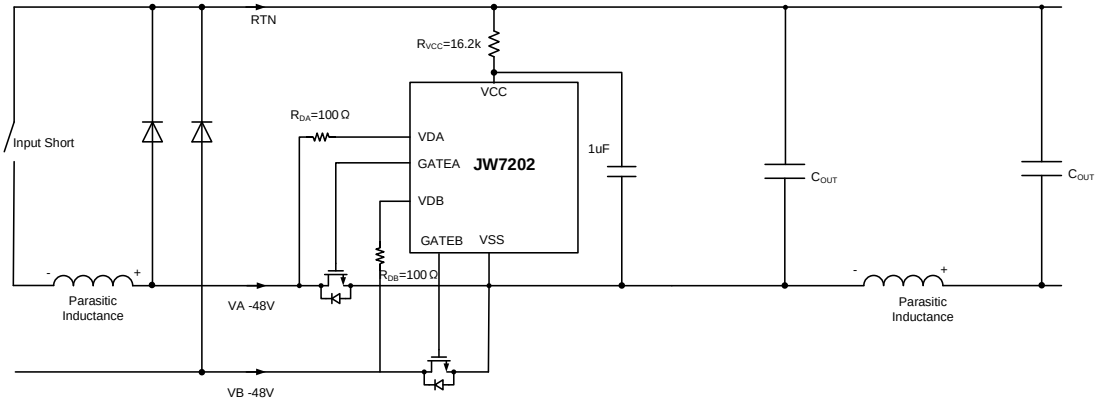


Figure 2 Input Supply Fault Transients

R_D Selection

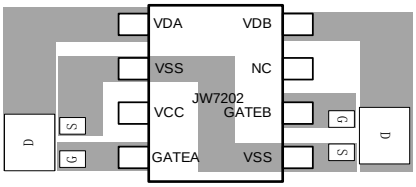
To protect V_{Dx} against negative voltage, it is recommended to add a resister between V_{Dx} pin and MOSFET drain. A 100Ω R_D prevents negative voltage spike of -1V and a 2kΩ R_D prevents negative voltage spike of -2V.

PCB Layout Note

The following advice should be considered when laying out a printed circuit board for the JW7202.

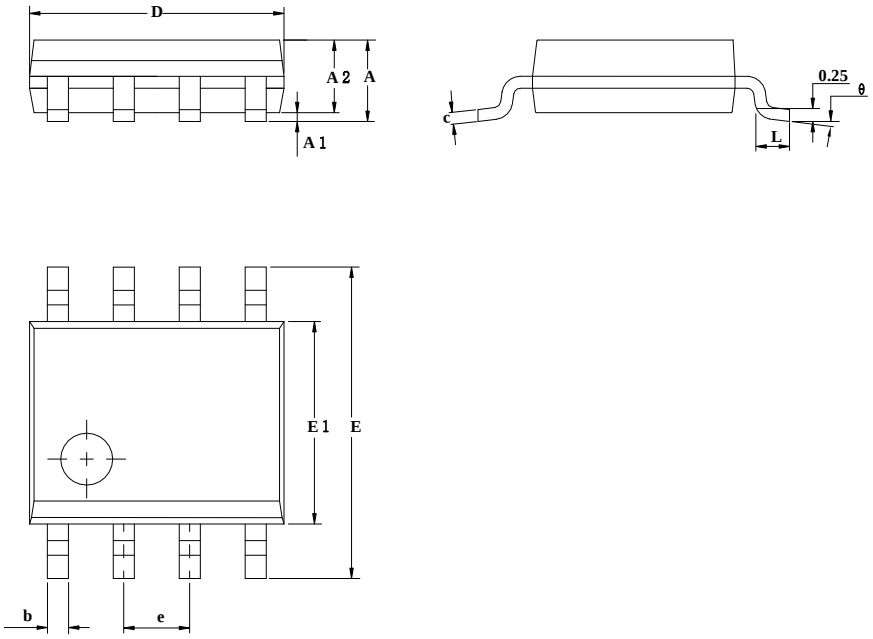
The inputs to the servo amplifiers, V_{Dx} and V_{SS} should be connected as closely as possible to the MOOSFET's terminals for good accuracy.

Keep the traces to the MOSFETs wide and short. The PCB traces associated with the power path through the MOSFETs should have low resistance. Use no-clean solder to minimize PCB contamination.



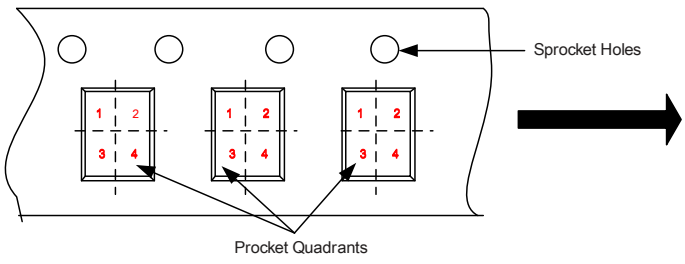
PACKAGE OUTLINE

SOP8 UNIT: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.32	0.42	0.52
c	0.10	0.20	0.30
D	4.50	5.00	5.50
E	5.50	6.00	6.50
E1	3.50	3.90	4.30
e	1.27TYP		
L	0.40	—	1.27
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
SOP8	1

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