JW7106

6A, 5.5V Low On-Resistance Single Channel Load Switch

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW®7106 is a low on-resistance single channel load switch with programmable turn-on rise time. It contains n-channel MOSFET that can provide 6A maximum continuous current. JW7106 can operate over an input voltage range of 0.8V to 5.5V.

In JW7106, a 220Ω load resistor is integrated for quick output discharge when load switch is turned off. The optional external capacitor connected to SS is used for output slew rate control.

JW7106 offers DFN2×2-8 package.

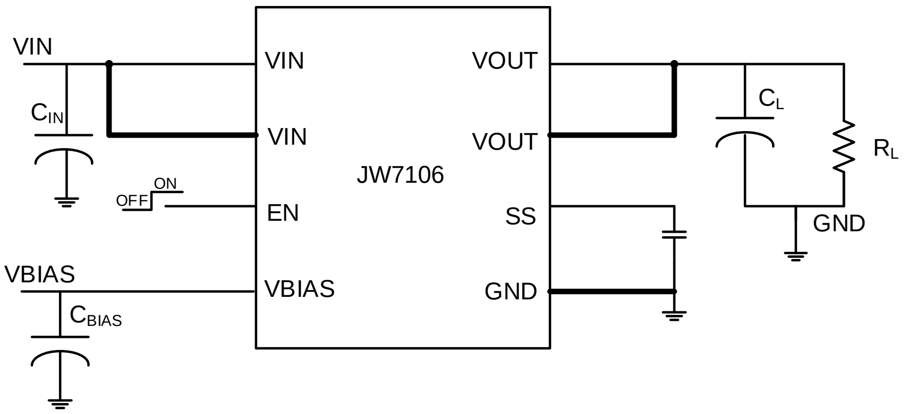
FEATURES

- Operating Range : 0.8V ~ 5.5V
  Low Quiescent Current (35uA)
- Low ON-Resistance
- Up to 6A Maximum Load Current
- Low-voltage Enable Control
- Externally Programmable Rise Time
- Quick Output Discharge
- Thermal Shutdown
- Available in DFN2×2-8 Package

APPLICATIONS

- Portable computers
- Tablet PCs
- Consumer Electronics
- Set-top Boxes and Residential Gateways
- Telecom Systems
- Solid-State Drives (SSD)

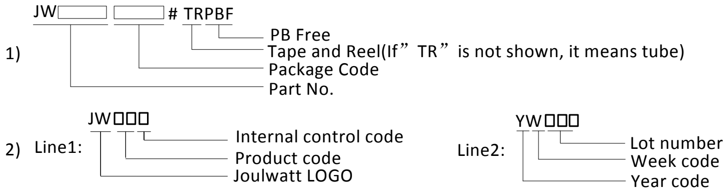
TYPICAL APPLICATION



ORDER INFORMATION

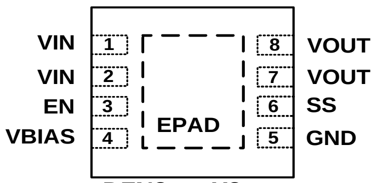
DEVICE[1]	PACKAGE	TOP MARKING[2]
JW7106DFND#TRPBF	DFN2X2-8	JWKD□ YW□□□

Notes:



PIN CONFIGURATION

TOP VIEW



DFN2mmX2mm

ABSOLUTE MAXIMUM RATING[1)]

VIN PIN Voltage .... -0.3V to 6V
VOUT PIN Voltage............ -0.3V to 6V
EN PIN Voltage............ -0.3V to 6V
SS PIN Voltage............-0.3V to Vout+6.5V
VBIAS Voltage ....-0.3V to 6V
Junction Temperature[2) 3)] 150ºC
Lead Temperature 260ºC
Storage Temperature ....-65ºC to +150ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS

VIN PIN Voltage .... 0.8V to V_{BIAS}
EN PIN Voltage .... 0V to 5.5V
VBIAS Voltage............2.5V to 5.5V
Operating Junction Temperature…............ -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
DFN2X2-8	120	34ºC/W

Note：

1) Exceeding these ratings may damage the device.
2) The JW7106 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
3) The JW7106 includes thermal protection that is intended to protect the device in overload conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = 5.0V, Typical values are for T_A = 25ºC, unless otherwise stated.

Symbol	Parameter	Condition		Min	Typ	Max	Units
POWER SUPPLIES AND CURRENTS							
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0mA V_{IN} = V_{EN} = VBIAS = 5.0V			35	60	uA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{EN}=0V, V_{OUT} =0V			0.1	1	uA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{EN}=0VV_{OUT} =0V	V_{IN} = 5.0V		0.1	1	uA
I_{EN}	EN pin input leakage current	V_{EN}= 5.5 V			0.1	1	uA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance (per channel)	I_{OUT} = -200mA VBIAS = 5.0V	V_{IN}= 5.0V		25	30	mΩ
			V_{IN}= 3.3V		25	30	
			V_{IN}= 1.8V		25	30	
			V_{IN}= 1.5V		25	30	
			V_{IN}= 1.2V		25	30	
			V_{IN}= 0.8V		25	30	
R_{PD}	Output pull-down resistance	V_{IN}=5.0V, V_{EN}=0V, I_{OUT} =15mA			220	300	Ω
V_{ENH}	EN high level voltage	V_{IN}=0.8V to 5V		1.2			V
V_{ENL}	EN low level voltage	V_{IN}=0.8V to 5V				0.5	V

V_{BIAS} = 2.5V, Typical values are for T_A = 25ºC, unless otherwise stated.

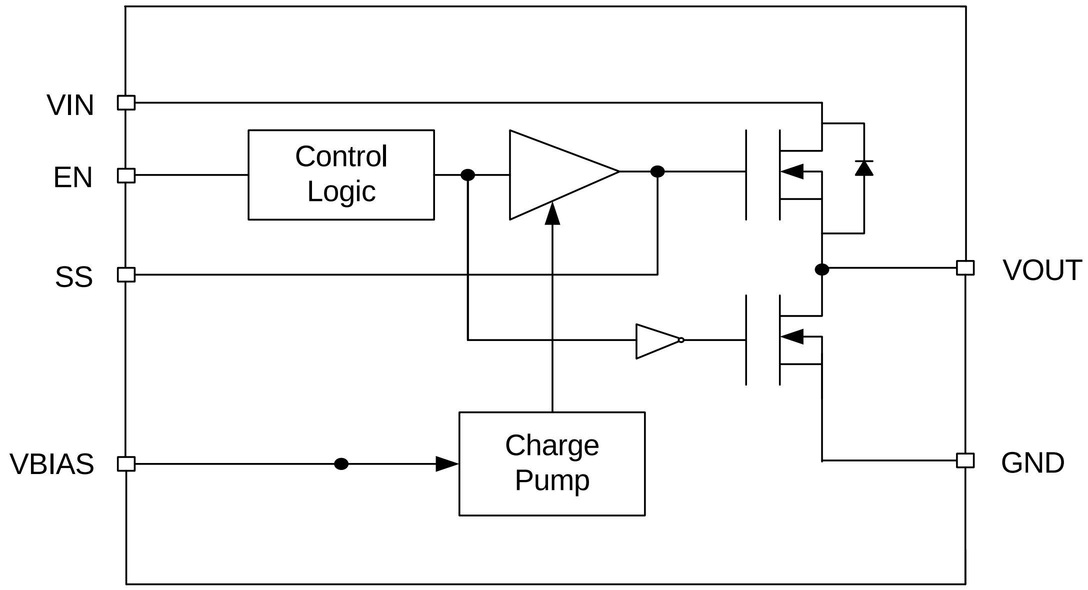
Symbol	Parameter	Condition		Min	Typ	Max	Units
POWER SUPPLIES AND CURRENTS							
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0mA V_{IN} = V_{EN} = VBIAS = 2.5V			26	55	uA
$I_{IN(VBIAS-OFF)}$	V_{EN}=0V, V_{OUT} =0V	V_{EN}=0V, V_{OUT} =0V			0.1	1	uA
$I_{IN(VIN-OFF)}$	$V_{IN1,2}$ off-state supply current	V_{EN}=0VV_{OUT} =0V	$V_{IN1,2}$ = 2.5V		0.1	1	uA
I_{EN}	EN pin input leakage current	V_{EN}= 5.5 V			0.1	1	uA
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance (per channel)	I_{OUT} = -200mA VBIAS = 5.0V	V_{IN}= 2.5V		28	33	mΩ
			V_{IN}= 1.8V		27	32	
			V_{IN}= 1.5V		27	32	
			V_{IN}= 1.2V		26	31	
			V_{IN}= 0.8V		26	31	
R_{PD}	Output pull-down resistance	V_{IN}=5.0V, V_{EN}=0V, I_{OUT} =15mA			240	320	Ω
OVER TEMPERATURE PROTECTION							
T_{SD}	Over Temperature Protection	V_{IN}=5.0V, V_{EN}=5V			155		℃
Hysteresis					25		℃

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IN} = V_{EN} = V_{BIAS}$ = 5 V, TA = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on Time	RL = 10Ω, CL = 0.1μF SS = 1nF		1268		μs
t_{OFF}	Turn-off Time			24		
t_R	V_{OUT} Rise Time			1509		
T_F	V_{OUT} Fall Time			22		
t_D	EN Delay Time			514		
V_{IN} = 0.8 V, $V_{EN} = V_{BIAS}$ = 5 V, TA = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on Time	RL = 10Ω, CL = 0.1μF SS = 1n F		470		μs
t_{OFF}	Turn-off Time			39		
t_R	V_{OUT} Rise Time			273		
T_F	V_{OUT} Fall Time			11		
t_D	EN Delay Time			333		
V_{IN} = 2.5 V, V_{EN} = 2.5 V, V_{BIAS} = 2.5 V, TA = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on Time	RL = 10Ω, CL = 0.1μF SS = 1n F		2001		μs
t_{OFF}	Turn-off Time			22		
t_R	V_{OUT} Rise Time			1977		
T_F	V_{OUT} Fall Time			18		
t_D	EN Delay Time			1012		
V_{IN} = 0.8 V, V_{EN} = 2.5 V, V_{BIAS} = 2.5 V, TA = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on Time	RL = 10Ω, CL = 0.1μF SS = 1n F		1166		μs
t_{OFF}	Turn-off Time			34		
t_R	V_{OUT} Rise Time			699		
T_F	V_{OUT} Fall Time			11		
t_D	EN Delay Time			817		

PIN DESCRIPTION

Pin	Name	Description
1、2	VIN	Switch input. Recommended voltage range for this pin is 0.8V to V_{BIAS} to obtain optimal on-resistance. Bypass capacitor is also need to minimize VIN dip during turn-on of the channel.
3	EN	Active high switch control input. Do not leave floating.
4	VBIAS	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
5	GND	Ground
6	SS	Slew rate control of switch. Capacitor connected to this pin should be rated no less than 15V.
7、8	VOUT	Switch output.
Thermal Pad		Thermal pad (exposed center pad) must be connected to GND.

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

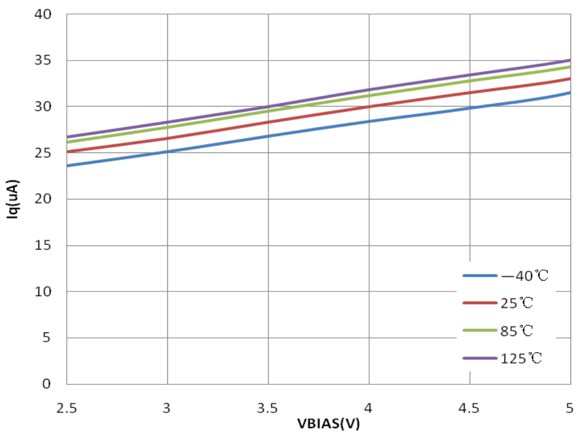


Fig.1. Quiescent Current vs. V_{BIAS}

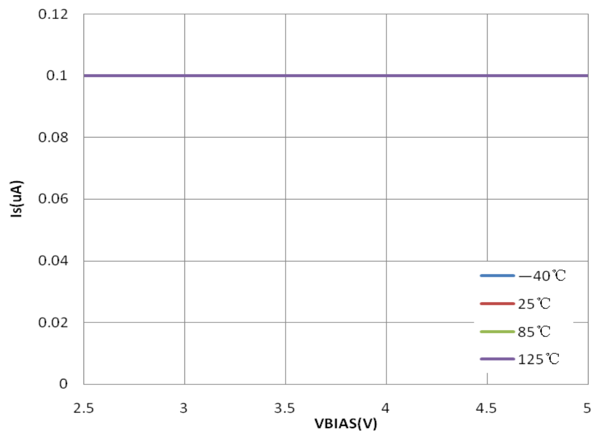


Fig.2. Shutdown Current vs. V_{BIAS}

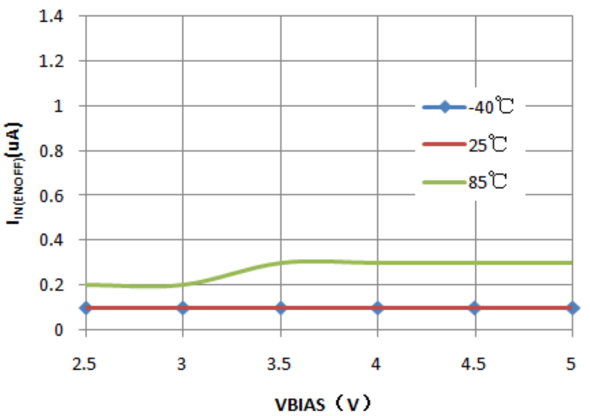


Fig.3. Off-State V_{IN} Current vs. V_{BIAS}

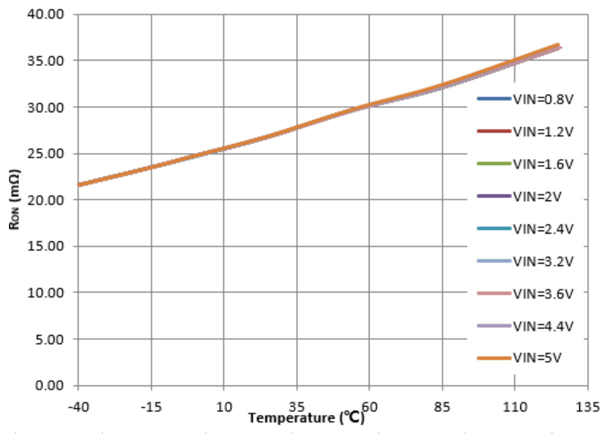


Fig.4. R_{ON} vs. Temperature (V_{BIAS} = 5 V)

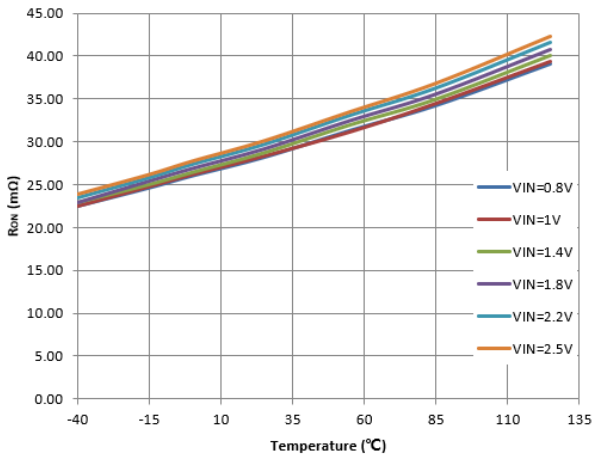


Fig.5. R_{ON} vs. Temperature (V_{BIAS} =2.5V)

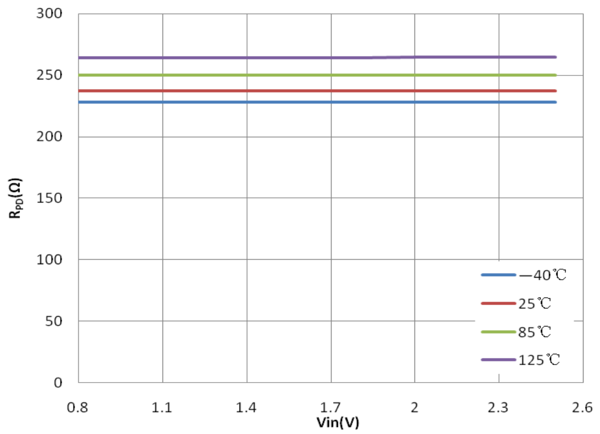


Fig.6. R_{PD} vs. V_{IN} (V_{BIAS} = 2.5 V)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

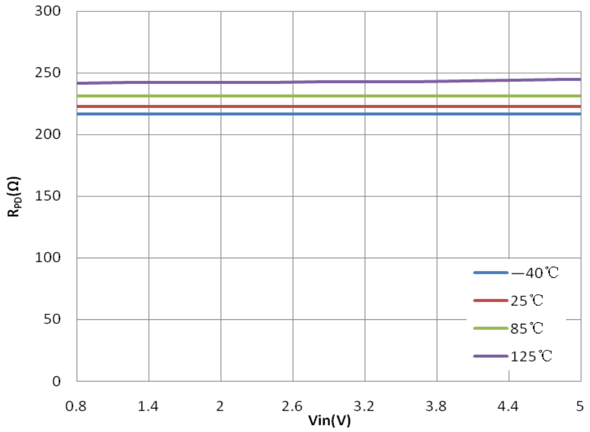


Fig.7. R_{PD} vs. V_{IN} (V_{BIAS} = 5 V)

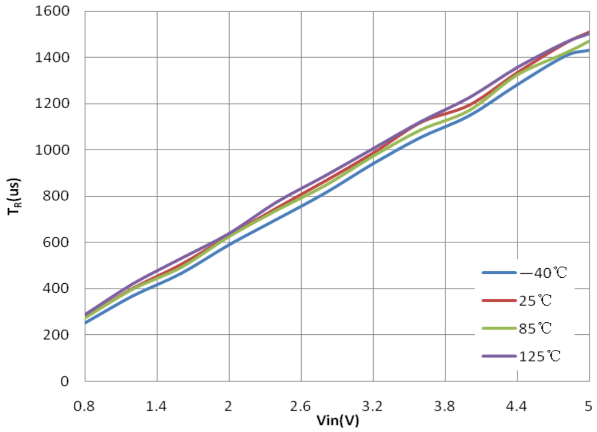


Fig.8. t_R vs. V_{IN} (V_{BIAS} = 5 V, SS = 1 nF)

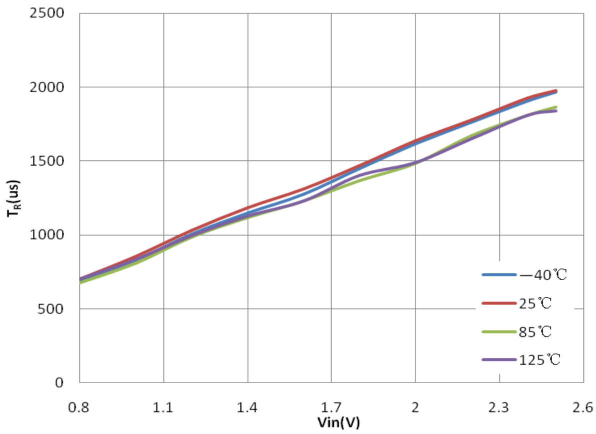


Fig.9. t_R vs. V_{IN} (V_{BIAS} = 2.5 V, SS = 1 nF)

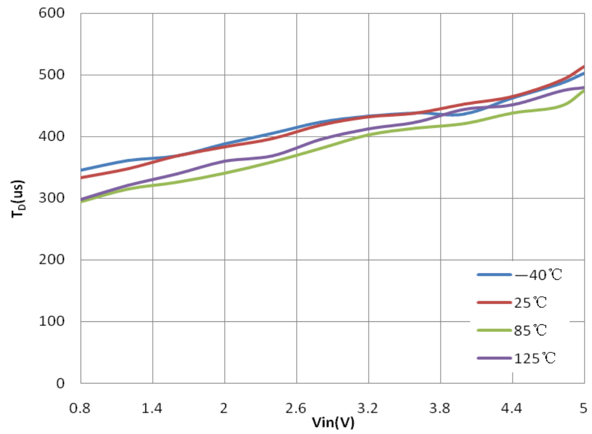


Fig.10. t_D vs. V_{IN} (V_{BIAS} = 5 V, SS = 1 nF)

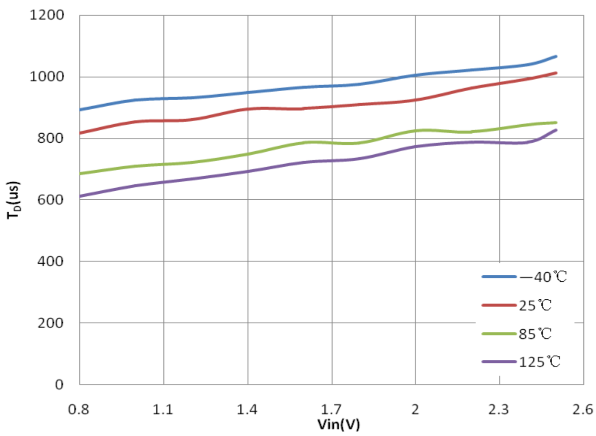


Fig.11. t_D vs. V_{IN} (V_{BIAS} = 2.5 V, SS = 1 nF)

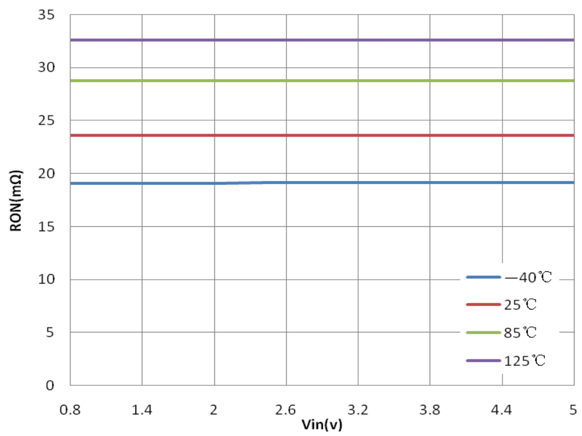


Fig.12. R_{ON} vs. V_{IN} (V_{BIAS} = 5 V)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

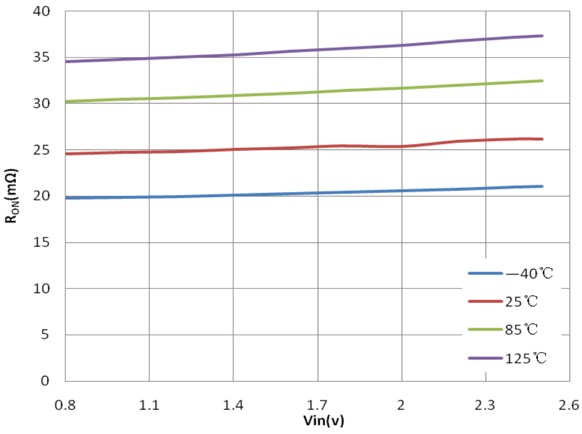


Fig.13. R_{ON} vs. V_{IN} (V_{BIAS} = 2.5 V)

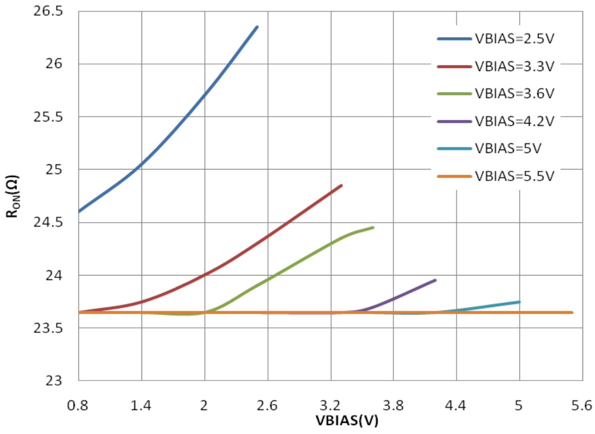


Fig. 14. R_{ON} vs. V_{BIAS} (TA = 25°C)

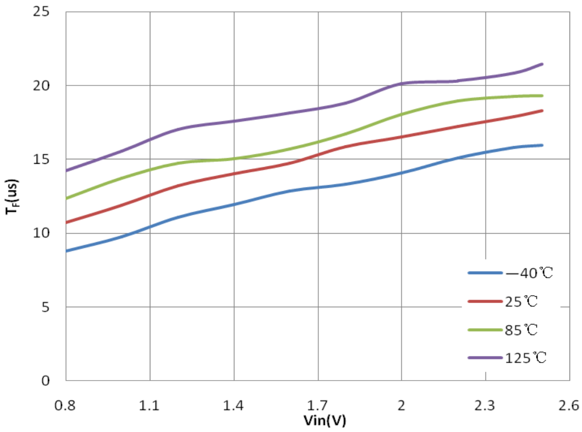


Fig.15. t_F vs. V_{IN}(V_{BIAS} = 2.5 V, SS = 1 nF)

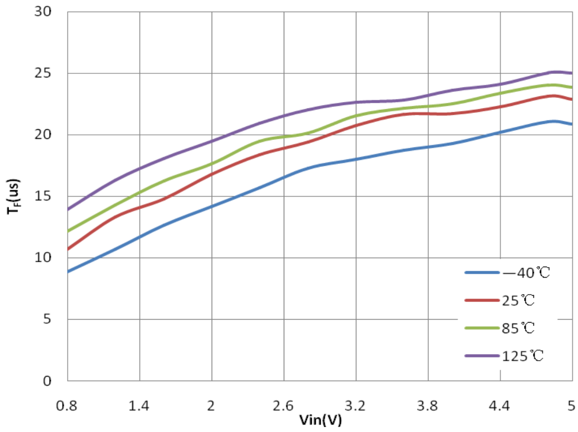


Fig.16. t_F vs. V_{IN}(V_{BIAS} = 5 V, SS= 1 nF)

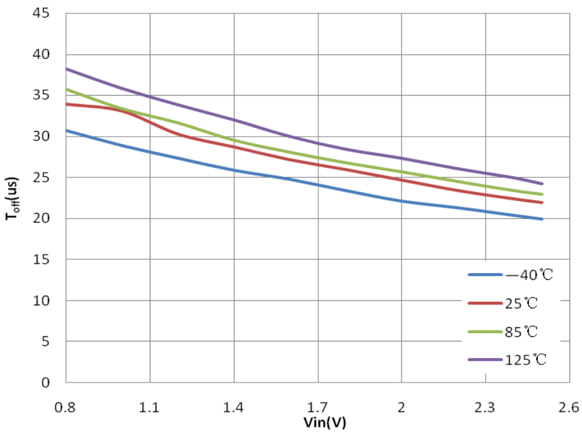


Fig.17. t_{OFF} vs. V_{IN}(V_{BIAS} = 2.5 V, SS = 1 nF)

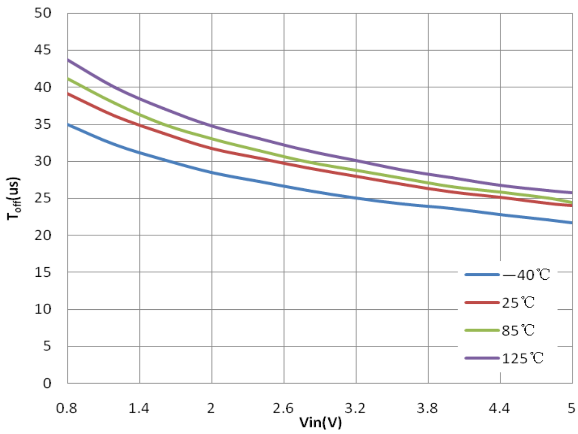


Fig. 18. t_{OFF} vs. V_{IN} (V_{BIAS} = 5 V, SS= 1 nF)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

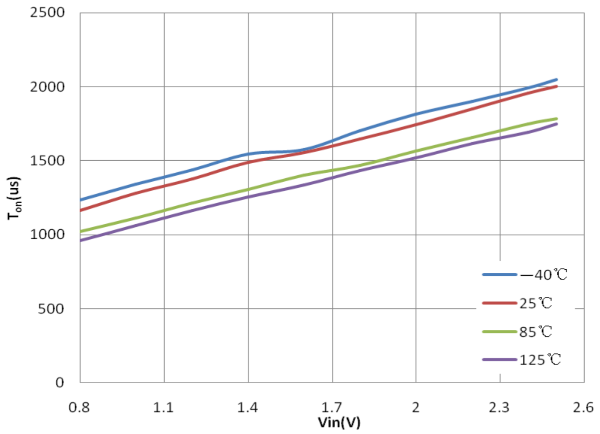


Fig.19. t_{ON} vs. V_{IN} (V_{BIAS} = 2.5 V, SS = 1 nF)

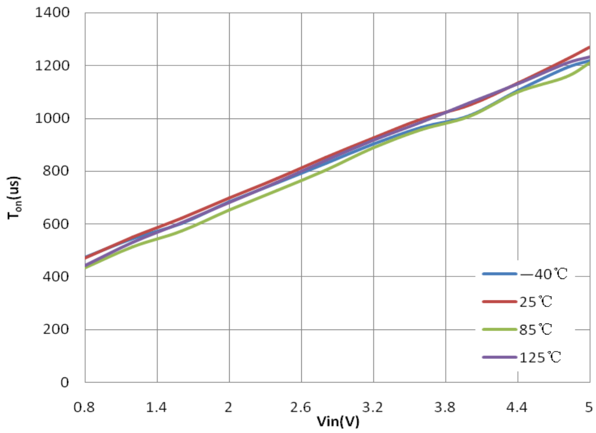


Fig.20. t_{ON} vs. V_{IN} (V_{BIAS} = 5 V, SS = 1 nF)

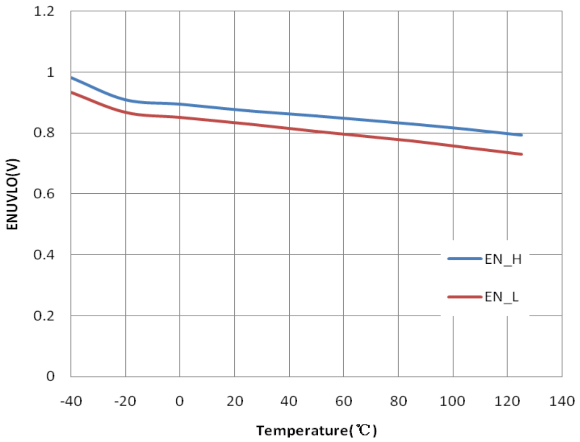


Fig.21. EN_UVLO vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A=25℃，C_{SS}=1nF

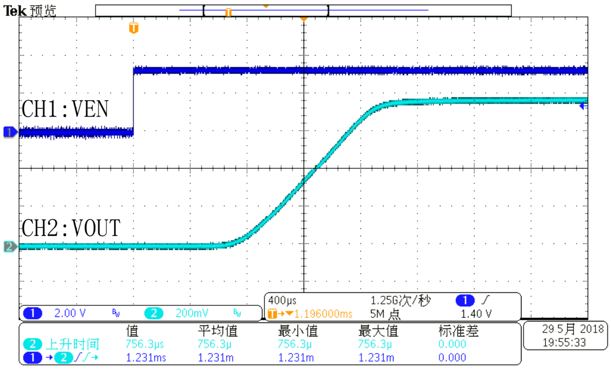


Fig. 22 Turn-on Response Time

(V_{IN} = 0.8V, V_{BIAS} = 2.5 V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

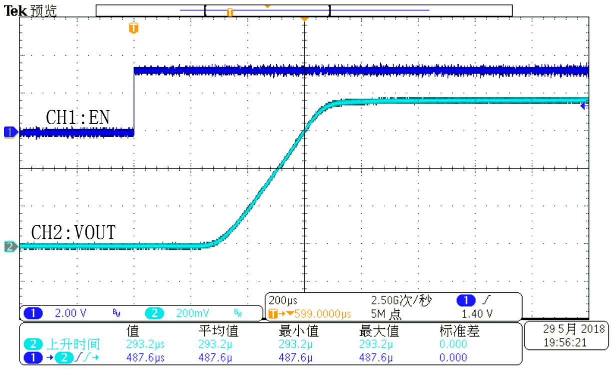


Fig.23 Turn-on Response Time

(V_{IN} = 0.8 V, V_{BIAS} = 5 V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

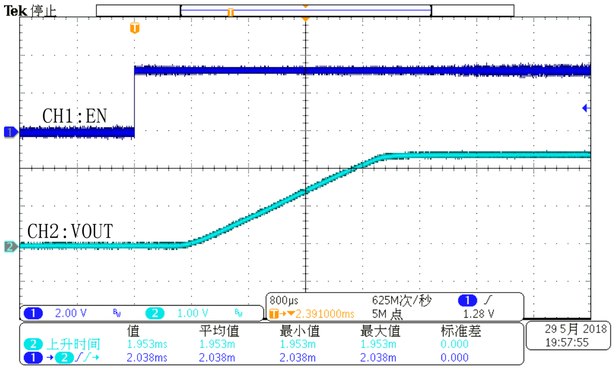


Fig. 24 Turn-on Response Time

(V_{IN} = 2.5V, V_{BIAS} = 2.5 V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

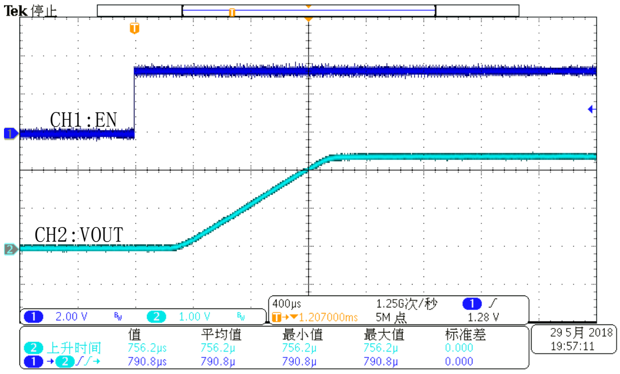


Fig.25 Turn-on Response Time

(V_{IN} = 5 V, V_{BIAS} = 5 V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

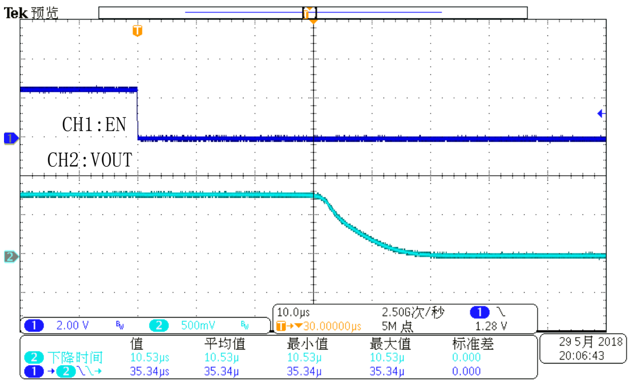


Fig.26 Turn-off Response Time

(V_{IN} = 0.8V, V_{BIAS} = 2.5V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

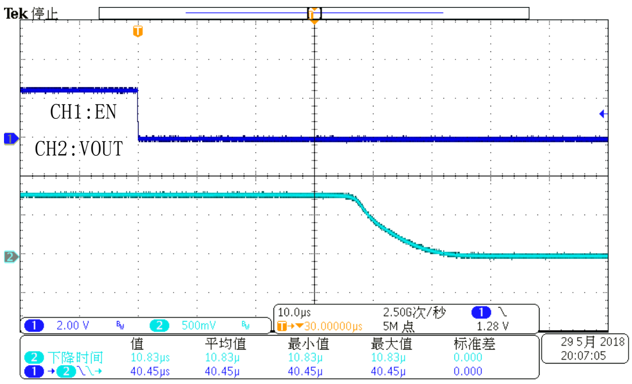


Fig. 27 Turn-off Response Time

(V_{IN} = 0.8V, V_{BIAS} = 5V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

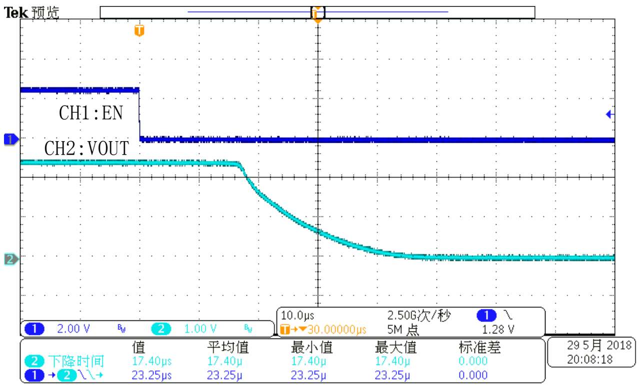


Fig.28 Turn-off Response Time

(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

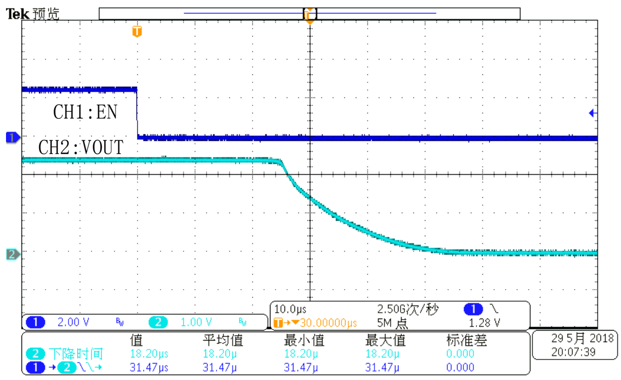


Fig. 29 Turn-off Response Time

(V_{IN} = 5V, V_{BIAS} = 5V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

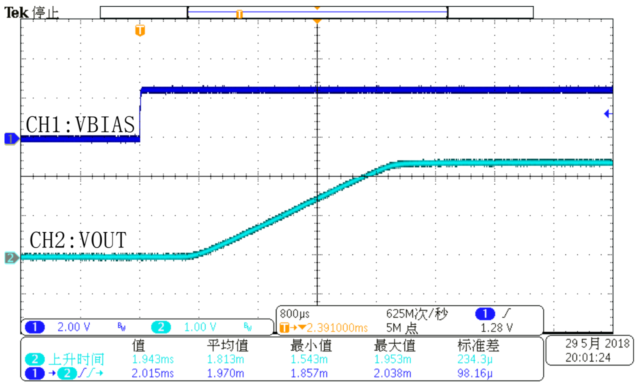


Fig.30 VBIAS Turn-on Response Time

(V_{IN} = 2.5V, V_{BIAS} = 2.5V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

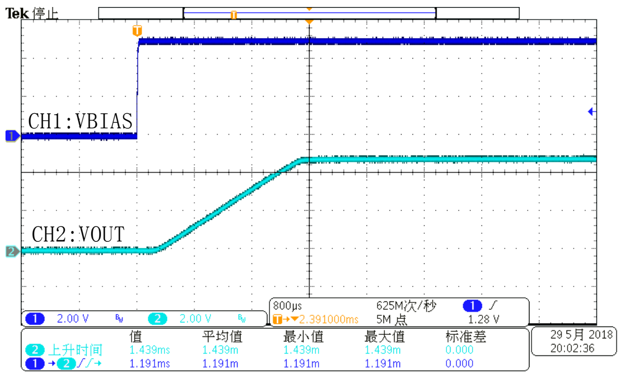
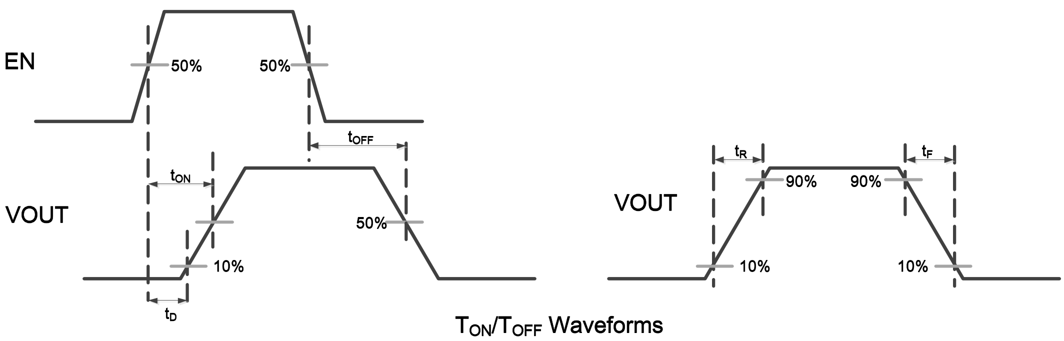


Fig. 31 VBIAS Turn-on Response Time

(V_{IN} = 5V, V_{BIAS} = 5V, C_{IN} = 1 μF, C_L = 0.1 μF, R_L = 10 Ω)

T Parameter Measurement Information



T_{ON}/T_{OFF} Waveforms

Rising and falling times of the control signal is 100ns.

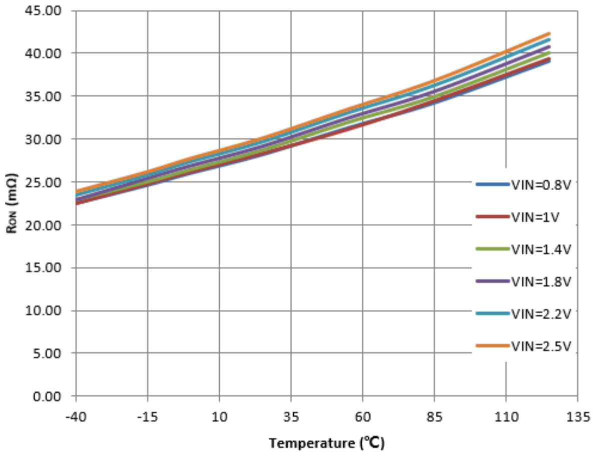
FUNCTIONAL DESCRIPTION

ON/OFF Control

EN high with 1.2V or high GPIO voltage enables the switch. The EN pin is compatible with standard logic threshold. This pin must be tied either high or low for proper functionality.

VIN and VBIAS Voltage Range

VBIAS is recommended to work within the range from 2.5V to 5.5V. For optimal on-resistance performance of load switch, make sure VIN ≤ VBIAS. Otherwise, the device could exhibit greater on-resistance than that in Electrical Characteristics. Resistance curves of a typical device at different temperature and VIN are shown as below.



Input Capacitor (Optional)

A 1-μF or higher ceramic capacitor is recommended to be placed between VIN and GND to reduce the voltage drop caused by inrush current when switch turns on to charge a full-discharged load capacitor. A higher values capacitor can further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to put an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

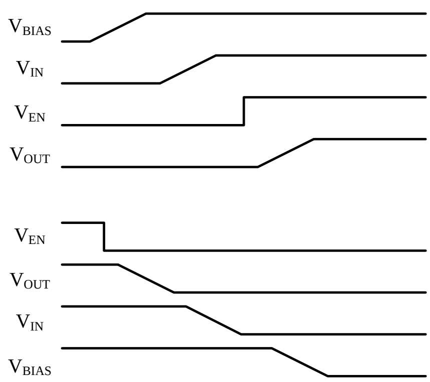
Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, an input capacitor greater than output capacitor is highly recommended. So the output can be discharged more quickly than input when the power supply is off. An input capacitor to output ratio of 10 to 1 is recommended. A larger output capacitor makes the initial turn-on transient smoother. In order to prevent the output from dropping, the output capacitor must be large enough to supply a fast transient load.

Over-Temperature Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults occurs. The JW7106 implements a thermal sensing circuit to monitor the operating junction temperature. Once the die temperature rises to approximately +155°C, the thermal protection feature activates as follows: The internal thermal sense circuitry turns the power switch off to prevent the power switch from damage. Once the junction temperature drops to 130°C, the MOSFET restart to work.

Power Sequencing



The charge pump block will stop working when Vbias is Low。The voltage of charge pump cannot discharge without Vbias. So EN shutdown before Vbias is recommended and also Vbias startup before EN and keep it high level is recommended.

PCB Guidelines

Good PCB helps improving the performance of JW7106:

1) For best performance, all traces should be as short as possible.
2) For best efficiency, the input and output decoupling capacitors should be placed as close to the device as possible, so that the parasitic impact can be minimized. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Device Functional Modes

En	VIN to VOUT	VOUT to GND
L	OFF	ON
H	ON	OFF

APPLICATION INFORMATION

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value. The inrush current presents a constant value controlled by the device. It can be calculated as below:

$$I_{inrush} = C \times dV/dt$$

Where,

C – output capacitance

dV – output voltage

dt – rise time

Take a 3.3V case as an example. The parameters are shown in the table.

DESIGN PARAMETER	VALUE
Input voltage	3.3V
Bias voltage	5V
Load capacitance (CL)	22μF
Maximum acceptable inrush current	400mA

To ensure an inrush current of less than 400 mA, choose a Css value that can-yield a rise time of more than 181.5μs.

JW7106 offers adjusted rise time for VOUT. So the user can control the inrush current during turn-on period. The appropriate rise time can be calculated using the following equation.

$$400\text{ mA} = 22\ \mu\text{F} \times 3.3\text{ V}/dt$$

$$dt = 181.5\ \mu\text{s}$$

Adjustable Rise Time

The rise time of JW7106 can be adjusted individually by external capacitors connected between SS and GND pins. To ensure desired performance, a capacitor with a minimum voltage rating of 15 V should be placed on the SS pin.

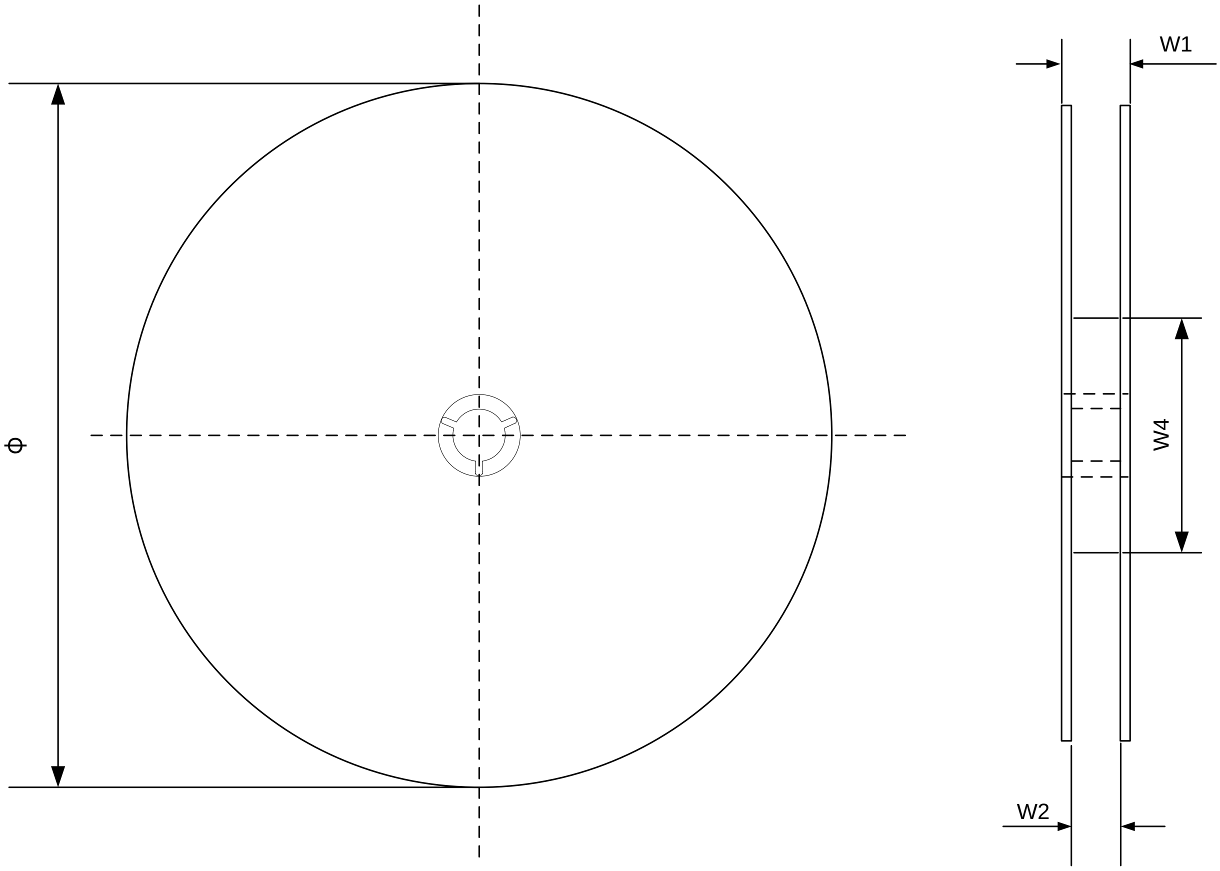
The approximate rise time of VOUT measured on a typical device at VBIAS = 5V is shown in table 1. Rise time can be calculated by multiplying the input voltage by the slew rate. Rise times shown below are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition, and the EN pin is used to enable the device.

Table1:

SS (pF)	RISE TIME (μs) 10% - 90%, CL = 0.1μF, CIN = 1μF, RL = 10Ω TYPICAL VALUES at 25°C, VBIAS = 5V, 25V X7R 10% CERAMIC CAP						
	0.8V	1.05V	1.5V	1.8V	2.5V	3.3V	5V
0	21	27	34	37	47	61	79
220	72	91	130	147	194	250	368
470	152	190	236	300	405	535	787
1000	286	365	462	588	803	1047	1582
2200	651	819	1138	1280	1823	2392	3574
4700	1234	1552	2180	2491	3520	4521	6768
10000	2303	2948	4139	4801	6638	8919	12900

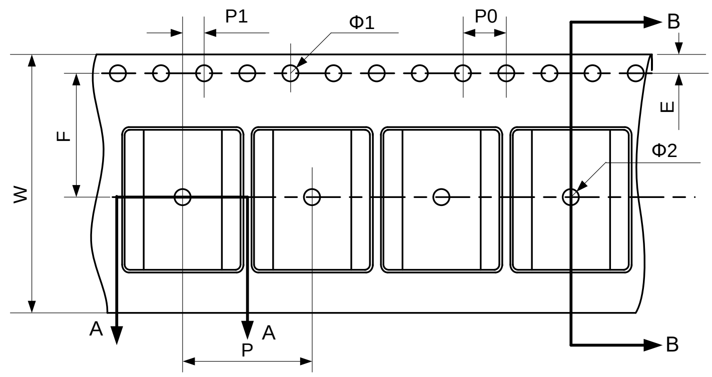
TAPE AND REEL INFORMATION

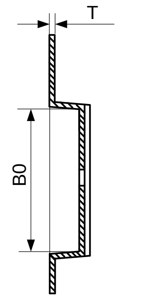
Reel



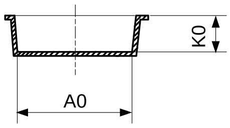
Package	Diameter Φ	Thickness W1	Width W2	W4
DFN2X2-8	178±2	12.30±2	9.5±2	60±2

Carrier Tape UNIT: mm





SECTION B-B



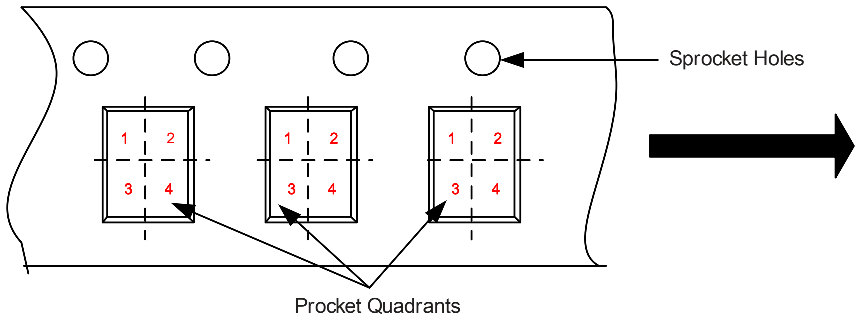
SECTION A-A

Note :

1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	P0	P1	P	A0	B0	W	T0	K0	Φ1	Φ2	E	F
DFN 2x2-8	4.00±0.10	2.00±0.10	4.00±0.10	2.30±0.20	2.30±0.20	8.00±0.30	0.25±0.20	1.00±0.35	1.50min	1.00min	1.75±0.10	3.50±0.10

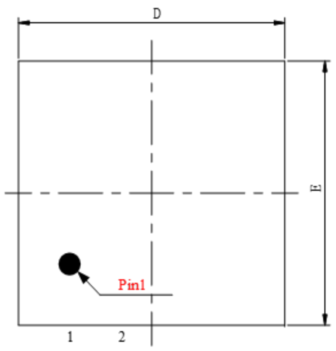
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



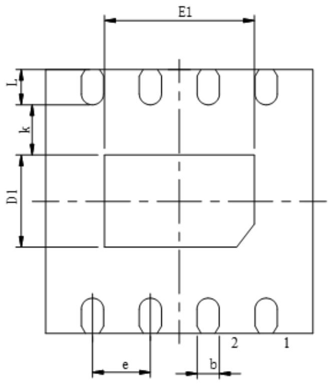
Package Type	Pin1 Quadrant
DFN2X2-8	2

PACKAGE OUTLINE

DFN2X2-8 UNIT: mm



TOP VIEW

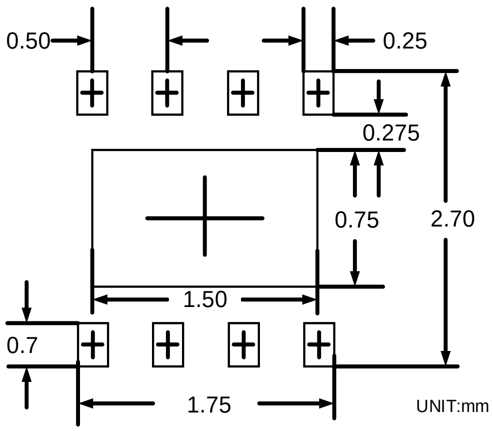


BOTTOM VIEW

SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	—	0.05
A3	0.20REF		
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	0.50	0.60	0.70
E1	1.10	1.20	1.30
k	0.35REF		
b	0.18	0.25	0.30
e	0.50BSC		
L	0.25	—	0.45

Minimum Footprint Layout Section



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