JW3312

Battery Protection IC For 3-5 Cells Battery Pack With Automatic Balance

DESCRIPTION

JW®3312 is a battery protection IC for the 3~5 cells rechargeable lithium-ion battery pack. JW3312 integrates high-accuracy voltage detection circuits, which realizes multiple protection functions including over-charge, over-discharge, over-current, over-temperature and VC5~VC0 pins open-wire.

FEATURES

- Wide range of operation voltage 5V to 35V
- Monitor 3~5 series battery pack
- High-accuracy voltage detection for each cell
  - Over-charge detection voltage V_{OC}: 3.6~4.5V (50mV step) ±25mV
  - Over-charge release hysteresis V_{OCRH}: 0V/0.1V/0.2V/0.35V
  - Over-discharge detection voltage V_{OD}: 2.1~3.1V (100mV step) ±50mV
  - Over-discharge release hysteresis V_{ODRH}: 0V/0.1~0.6V (100mV step)
- Discharge over-current detection in 3-step
  - 1st detection voltage V_{DOI1}: 0.050~0.25V (50mV step) ±10mV
  - 2nd detection voltage V_{DOI2}:
  - 0.1~0.5V (100mV step) ±20mV
  - Short circuit detection voltage V_{SHT}: 0.1~1.0V (100mV step) ±80mV
- Charge over-current detection voltage V_{COI}:
  - 0.015~0.155V (10mV step) ±10mV

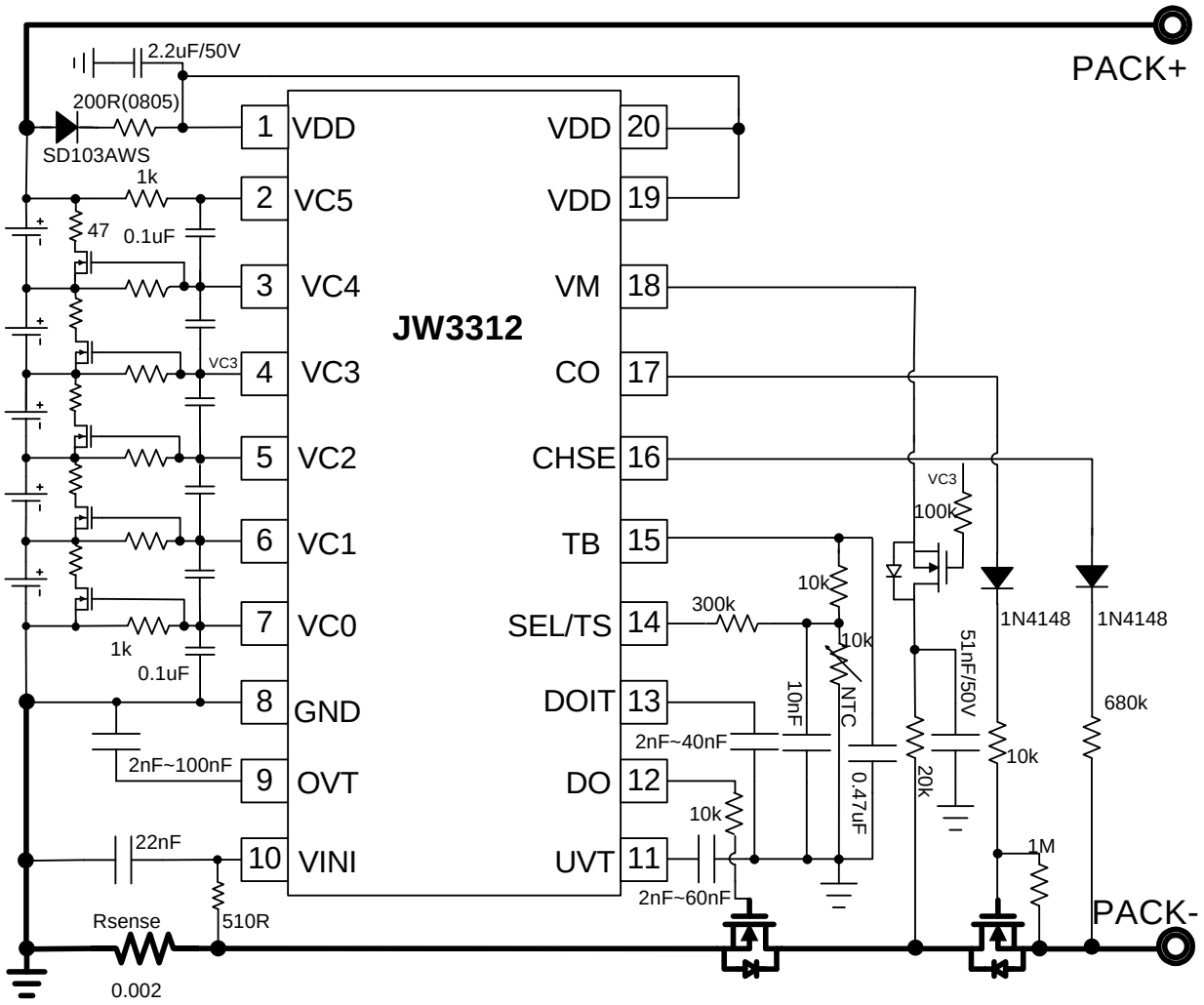
- Fixed internally:
  Load short circuit detection delay time t_{SHT}: 300μs
  Charge over-current detection delay time t_{COI}: 1s
- Programmable by external capacitor
  - Discharge over-current detection delay time t_{DOI}:
    1st: 0.1s~2s 2nd: (0.1~2s)×0.1
  - Over-discharge detection delay time t_{OD}: 0.1s~3s
  - Over-charge detection delay time t_{OC}: 0.1s~5s
- Balance function:
  Level-1 bleeding threshold voltage V_{BAL1}: V_{OC}-225mV~V_{OC}-25mV (25mV step) ±25mV
  Level-2 bleeding threshold voltage V_{BAL2}: V_{OC}/V_{OC}-25mV/V_{OC}-50mV ±25mV
- High-accuracy battery temperature detection
- Provide passive balance
- Provide VC5~VC0 open-wire detection
- Wide range of operation temperature -40°C to +85°C
- Low current consumption (T=25°C)
  Full power mode 15μA Typ.
  Sleep mode 3μA Typ.
  Shutdown mode 350nA Typ.
- 20-Pin TSSOP

APPLICATIONS

- Rechargeable lithium-ion battery pack
- Power tool
- UPS backup battery

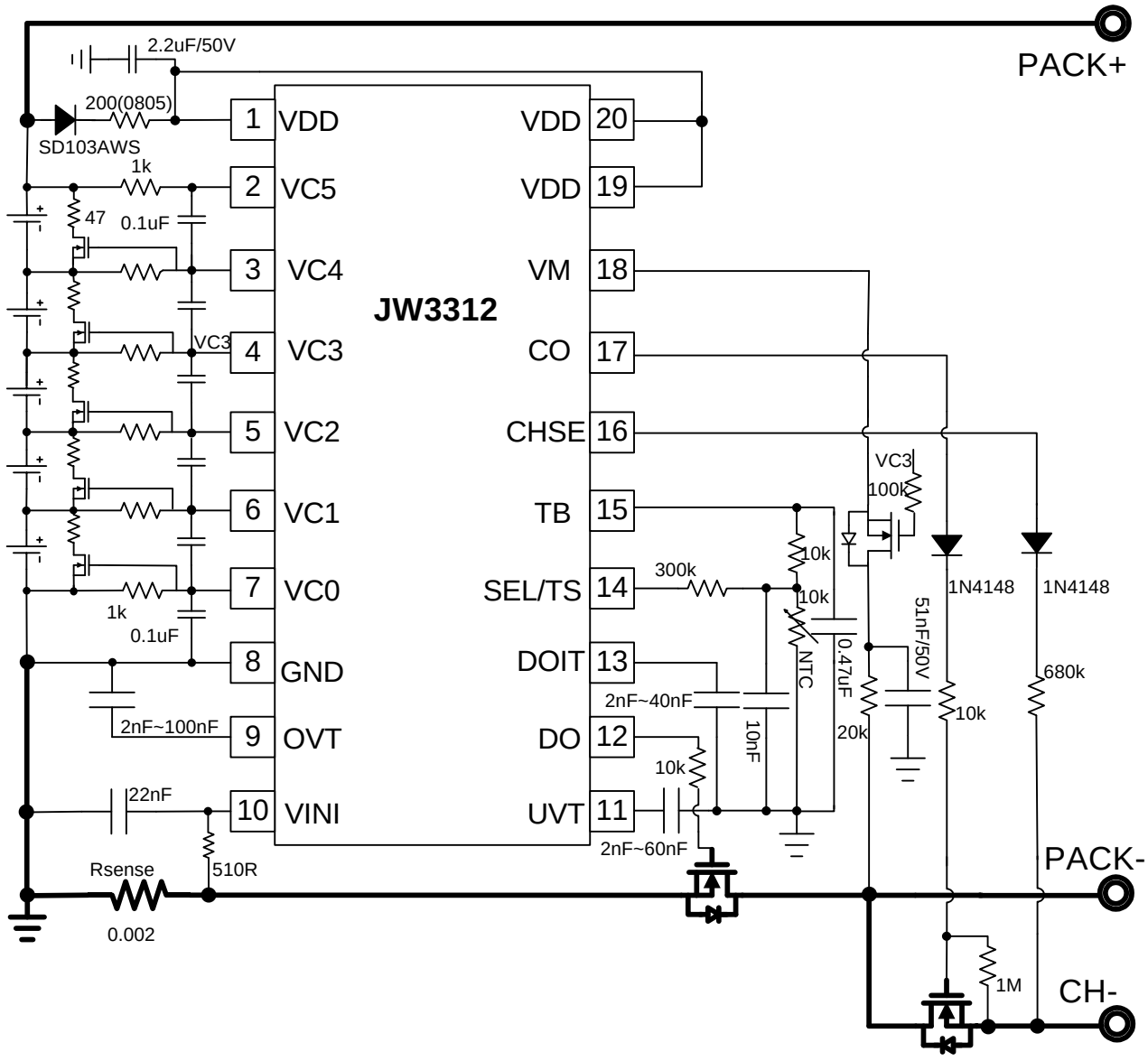
TYPICAL APPLICATION

One PACK- PORT (5cells)



TYPICAL APPLICATION

PACK- CH- separated (5cells)



Selection Guides

Production name structure

JW3312-XXX

Digital code*[1]
Balance function need or not

Series code*[2]
Sequentially set from AA to ZZ

1. Balance function need or not: X→ No need, Y→ Need
2: Product Series List, relates to different detection threshold voltage

Products Series List

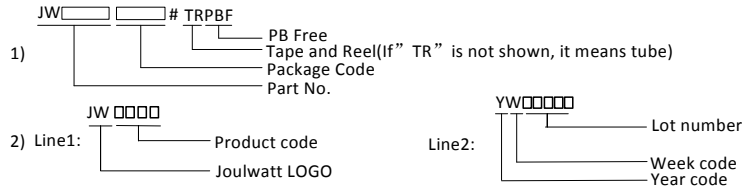
Type/Item	Over -charge detection voltage [V_{OC}]	Over -charge release voltage [V_{OCL}]	Over -discharge detection voltage [V_{OD}]	Over -discharge release voltage [V_{ODH}]	Charge over -current detection voltage [V_{COI}]	Discharge over-current 1 detection voltage [V_{DOI1}]	Discharge over-current 2 detection voltage [V_{DOI2}]	Short circuit detection voltage [V_{SHT}]	Balance detection voltage [V_{BAL1}]
JW3312-AAY	4.2V	4.1V	2.8V	3.0V	25mV	100mV	200mV	400mV	4.175V
JW3312-ABY	4.25V	4.15V	2.7V	3.0V	25mV	100mV	200mV	400mV	4.225V
JW3312-ACY	4.25V	4.15V	2.7V	3.0V	25mV	100mV	200mV	300mV	4.225V
JW3312-PAY	3.85V	3.75V	2.2V	2.5V	35mV	150mV	200mV	400mV	3.625V
JW3312-NBY	4.25V	4.15V	2.7V	3.0V	disable	100mV	200mV	400mV	4.225V
JW3312-PBY	3.7V	3.6V	2.1V	2.4V	65mV	100mV	200mV	500mV	3.5V
JW3312-ADY	4.20V	4.05V	2.8V	3.0V	15mV	100mV	200mV	400mV	4.0V
JW3312-AEY	4.25V	4.15V	2.7V	3.0V	25mV	100mV	200mV	400mV	4.075V

Remark: *Please contact our sales office for products with detection voltage values other than those specified above.*

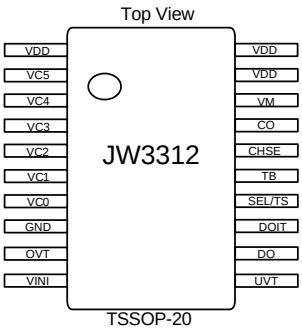
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW3312-AAYTSSOPC#TRPBF	TSSOP20	JW3312-AAY YW□□□□□
JW3312-ABYTSSOPC#TRPBF	TSSOP20	JW3312-ABY YW□□□□□
JW3312-ACYTSSOPC#TRPBF	TSSOP20	JW3312-ACY YW□□□□□
JW3312-PAYTSSOPC#TRPBF	TSSOP20	JW3312-PAY YW□□□□□
JW3312-NBYTSSOPC#TRPBF	TSSOP20	JW3312-NBY YW□□□□□
JW3312-PBYTSSOPC#TRPBF	TSSOP20	JW3312-PBY YW□□□□□
JW3312-ADYTSSOPC#TRPBF	TSSOP20	JW3312-ADY YW□□□□□
JW3312-AEYTSSOPC#TRPBF	TSSOP20	JW3312-AEY YW□□□□□

Note：



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

VDD,VC5,VC4,VC3,VC2,.....-0.3V to +40V
VC1.....-0.3V to +28V
VC0.....-0.3V to +8V
DO, VM.....-0.3V to +15V
CO.....-18V to 15V
UVT, SEL/TS, DOIT, VINI, OVT, TB, CHSE..... -0.3V to +6.5V
Battery cell voltage VC(n)-VC(n-1).....-0.3V to 12V
Junction Temperature[2)]..... 150ºC
Lead Temperature 260ºC
Storage Temperature .....-65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS

Junction Temperature (T_J)..... -40ºC to 125ºC
VC(N)-VC(N-1) ..... 2V to 5V
VDD to GND ..... 5V to 35V

THERMAL PERFORMANCE[3)]

	θ_{JA}	θ_{JC}
TSSOP20	98.4	37ºC/W

Note:

1) Exceeding these ratings may damage the device.

2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

TA = 25ºC, unless otherwise stated.

Item		Symbol	Condition	Min.	Typ.	Max.	Units
Power supply							
Operation voltage between VDD pin and GND pin		V_{DSOP}		5		35	V
Power-on reset threshold		V_{PON}		4.5	4.8	5.1	V
Shutdown threshold		V_{PDOWN}		4.2	4.5	4.8	V
Current consumption during full power		I_{FP}			15	20	μA
Current consumption during sleep		I_{SLEEP}			3	6	μA
Current consumption during shutdown		$I_{SHUTDOWN}$			350		nA
Voltage/Current Protections Threshold Voltage							
Detection period time for voltage		t_{DETV}	Full power mode		0.5		s
		t_{DETV_SLP}	Sleep mode		2		s
Over-charge	Protection threshold	V_{OC}		V_{OC}-0.025	V_{OC}	V_{OC}+0.025	V
	Release threshold	V_{OCL}		V_{OCL}-0.04	V_{OCL}	V_{OCL}+0.04	V
	Protection delay time	t_{OC} [4)]		70%t_{OC}	t_{OC}	130%t_{OC}+ t_{DETV}	s
		t_{OCS} [4)]	OVT pin short to GND	64	-	164	ms
		t_{OCO} [4)]	OVT pin open	0	-	100	ms
Over-discharge	Protection threshold	V_{OD}		V_{OD}-0.05	V_{OD}	V_{OD}+0.05	V
	Release threshold	V_{ODH}		V_{ODH}-0.07	V_{ODH}	V_{ODH}+0.07	V
	Protection delay time	t_{OD} [4)]		70%t_{OD}	t_{OD}	130%t_{OD}+ t_{DETV}	s
		t_{ODS} [4)]	OVT pin short to GND	64	-	164	ms
		t_{ODO} [4)]	OVT pin open	0	-	100	ms
Charge over- current	Protection threshold	V_{COI}		V_{COI}-10	V_{COI}	V_{COI}+10	mV
	Protection delay time	t_{COI} [4)]		0.7	1	1.3	S
Discharge over-current	1st protection voltage	V_{DOI1}		V_{DOI1}-10	V_{DOI1}	V_{DOI1}+10	mV
	1st protection delay time	t_{DOI1} [4)]		70%t_{DOI1}	t_{DOI1}	130%t_{DOI1}	ms
		t_{DOI1S} [4)]	DOIT pin short	64	-	164	ms

			to GND				
		t_{DOI1O}[4]	DOIT pin open	0	-	100	ms
	2nd protection voltage	V_{DOI2}		V_{DOI2}-20	V_{DOI2}	V_{DOI2}+20	mV
	2st protection delay time	t_{DOI2}[4]		7%t_{DOI1}	10%t_{DOI1}	13%t_{DOI1}	ms
	Short protection voltage	V_{SHT}		V_{SHT}-80	V_{SHT}	V_{SHT}+80	mV
	Short protection delay time	t_{SHT}[4]		150	300	450	μs
Temperature Protection Threshold Voltage							
Detection period time for temperature		t_{DETT}			2		s
		t_{DETT_SLP}			8		s
Detection effective time for temperature		t_{EFF_DETT}			3		ms
Charge temperature protection	Over-temperature protection threshold	V_{COT}	50°C±4°C R_{NTC}=103AT	28.58%	29.58%	30.58%	V_{TB}
	Over-temperature release hysteresis	V_{COTRH}	5°C		3.33%		V_{TB}
	Under-temperature protection threshold	V_{CUT}	0°C±4°C R_{NTC}=103AT	72.33%	73.33%	74.33%	V_{TB}
	Under-temperature release hysteresis	V_{CUTRH}	5°C		4.58%		V_{TB}
	protection delay time	t_{COT}[4]		3.5	4	6.5	s
Discharge temperature protection	Over-temperature protection threshold	V_{DOT}	70°C±4°C R_{NTC}=103AT	17.33%	18.33%	19.33%	V_{TB}
	Over-temperature release hysteresis	V_{DOTRH}	10°C		5%		V_{TB}
	Under-temperature protection threshold	V_{DUT}	-20°C±4°C R_{NTC}=103AT	86.08%	87.08%	88.08%	V_{TB}
	Under-temperature release hysteresis	V_{DUTRH}	10°C		6.25%		V_{TB}
	protection delay time	t_{DOT}[4]		3.5	4	6.5	s
State detection	Discharge detection	V_{TH_DSG}		2	4	6	mV

	threshold						
	Charge detection threshold	V_{TH_CG}		-6	-4	-2	mV
Balance Function							
Level-1 Bleeding threshold voltage		V_{BAL1}		V_{BAL1}-0.025	V_{BAL1}	V_{BAL1}+0.025	V
Level-2 bleeding threshold voltage		V_{BAL2}		V_{BAL2}-0.025	V_{BAL2}	V_{BAL2}+0.025	V
Level-1 allowance bleeding deviation voltage between high voltage battery and low voltage battery		$\triangle V_{B\_ALLOW}$		15	40	65	mV
Bleeding resistor[5]		R_{BAL}			50		Ω
Balance period time		t_B			0.5		s
Bleeding delay time[4]		t_{BAL_DELAY}			30		ms
Odd cells bleeding time[4]		t_{B_ODD}			200		ms
Even cells bleeding time[4]		t_{B_EVEN}			200		ms
Cell balancing relaxation time before cell voltage measured[4]		t_{B_RELAX}			100		ms
VCN Open-Wire Detection							
VCN open-wire detection cycle		t_{OPEN}			2		s
3/4/5 Cells Application Configuration							
SEL/TS pin source current[4]		I_{SEL}			5		μA
3 Cells configuration comparator threshold voltage[4]		V_{SEL0}	Recommend R_{SEL}=0R			100	mV
4 Cells configuration comparator threshold voltage[4]		V_{SEL1}	Recommend R_{SEL}=100K	300		600	mV
5 Cells configuration comparator threshold voltage[4]		V_{SEL2}	Recommend R_{SEL}=300K	900			mV
Output Voltage							
CO output voltage L		V_{COL}			High-Z		V
CO output voltage H		V_{COH}	Full power mode	10	12	15	V
			Sleep mode	4	4.5		V
DO output voltage L		V_{DOL}		0	0	0.5	V
DO output voltage H		V_{DOH}		10	12	15	V
Input Current							

VCn pin current(n=0~5)	I_{VCn}		-1		1	μA
Output Current						
CO pin maximum source current[4)]	I_{COH}		2	4	6	mA
DO pin maximum source current[4)]	I_{DOH}		3	5	7	mA
DO pin maximum sink current[5)]	I_{DOL}		70	100	110	mA
Load Detection						
Resistance between VM pin and GND pin	R_{VM}		20	40	60	kΩ
Load detection threshold	V_{VMD}		0.8	1	1.2	V
Charger Detection						
Charger detection pull up current	I_{PU}		2.7	3	3.3	μA
Charger detection threshold	V_{CHSE}		3.3	3.6	3.9	V

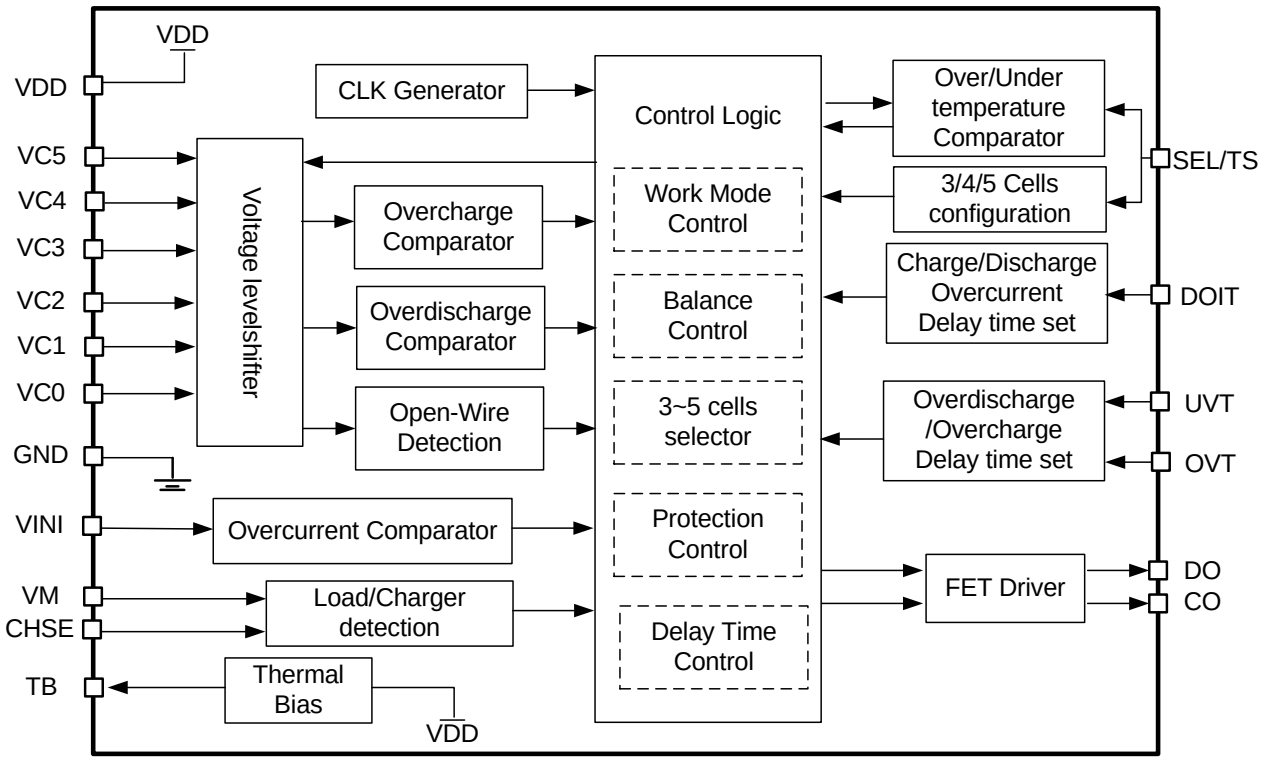
Notes:

4) Guaranteed by design.

PIN DESCRIPTION

Pin No.	Name	Description
1, 19, 20	VDD	Input pin for positive power supply
2	VC5	Connection pin for battery5's positive voltage
3	VC4	Connection pin for battery 4's positive voltage
4	VC3	Connection pin for battery 3's positive voltage
5	VC2	Connection pin for battery 2's positive voltage
6	VC1	Connection pin for battery 1's positive voltage
7	VC0	Connection pin for battery 1's negative voltage
8	GND	Input pin for negative power supply
9	OVT	Over-charge protection delay time setting
10	VINI	Charge and discharge over-current detection terminal
11	UVT	Over-discharge protection delay time setting
12	DO	Gate connection pin for discharge control MOSFET
13	DOIT	Discharge over-current delay time setting pin
14	SEL/TS	This is a dual-purpose Pin (1) Thermal sense input (2) 3/4/5 cells selection terminal
15	TB	Thermal bias output
16	CHSE	Charger detection pin
17	CO	Gate connection pin for charge control MOSFET
18	VM	Load detection Pin

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Normal Status

In the JW3312, both CO and DO pins output high level voltage when all battery voltages are between V_{OD} and V_{OC}, the battery temperature is between V_{COT} and V_{CUT}, and the VINI pin voltage is less than V_{DOI1}. This is the normal status.

Over-charge Status

JW3312 detects cell voltage once per t_{DETV}. When any battery voltage increases to V_{OC} or more for longer than t_{OC}, the CO pin outputs high-Z. Since the CO pin pulled down to the PACK- voltage by an external resistor, the charge MOSFET is turned off to stop charging. This is the over-charge status.

The over-charge status is released if either of the conditions mentioned below is satisfied:

(1) The battery voltage drops to V_{OCL} or less.

(2) The VINI pin voltage is higher than V_{TH_DSG} and all battery voltage drops to V_{OC}.

Over-discharge Status

JW3312 detects cell voltage once per t_{DETV}. When any voltage of batteries decreases to V_{OD} or lower for longer than t_{OD}, the DO pin outputs low level voltage. The discharge MOSFET is turned off and discharge stops. This is the over-discharge status.

When discharge MOSFET is off, VM pin is pulled down to the GND level via R_{VMS} internally. To reduce power consumption, the IC will entry sleep mode and CO pin outputs 4.5V. The IC will wake up to over-discharge status every 2s. The sleep status will not enter if the VINI pin voltage higher than V_{TH_CG}.

The over-discharge status is released if either condition mentioned below is satisfied:

(1) The VM pin voltage is lower than V_{VMD}, and the battery voltage increases to V_{ODH} or more.

(2) The VM pin voltage is lower than V_{VMD}, and the VINI pin voltage is lower than V_{TH_CG} during charging.

Discharge Over-current Status

In the JW3312, if the VINI pin voltage increases to V_{DOI} or more (discharge over-current threshold voltage) for longer than t_{DOI} (discharge over-current detection delay time), the DO pin outputs low level voltage. The discharge MOSFET is turned off and discharge stops. This is the discharge over-current status.

The VM pin is pulled down to the GND level via R_{VMS} internally.

JW3312 has three levels for discharge over-current detection (V_{DOI1}, V_{DOI2}, V_{SHT}). The JW3312 actions against load short circuit detection voltage (V_{SHT}) are as well in V_{DOI}.

The discharge over-current status is released if the following condition is satisfied.

The VM pin voltage is lower than V_{VMD}.

Charge Over-current Status

If the VINI pin voltage increases to V_{COI} or more for longer than t_{COI}, the DO pin outputs low level voltage and the CO pin outputs high-Z. The charge and discharge MOSFETs are turned off. This is the charge over-current status.

The CHSE pin is pulled up to the 5V regulator via I_{PU} internally.

The charge over-current status is released if the following condition is satisfied:

The CHSE pin voltage is higher than V_{CHSE}

Delay Time Setting

In the discharge over-current and over-discharge detection, users are able to set the delay time through an external capacitor.

Take the discharge over-current detection for example, when the VINI pin voltage reaches V_{DOI1} or more, JW3312 starts charging C_{DOIT} (the DOIT pin capacitor) via I_{DOIT} (the DOIT pin output current). After a certain period, the DO pin outputs low level voltage. This period is t_{DOI1}, which can be calculated using the following equation.

$t_{DOI1}[s]= n \times \Delta V \times C_{DOIT}[nF] / I_{DOIT} [\mu A]$

$= 400(typ.) \times C_{DOIT}[nF] /8[\mu A]$ (typ.)

$= 50[M\Omega](typ.) \times C_{DOIT}[nF]$

In case C_{DOIT}=2nF, t_{DOI1} is calculated as follows.

t_{DOI1} [s] = 50[MΩ](typ.)× 2[nF] = 0.1 [s] (typ.)

The 2nd discharge over-current detection delay time (t_{DOI2}) is calculated as below.

$t_{DOI2}=t_{DOI1}\times 0.1$

The function of over-discharge detection delay time is same to the discharge over-current detection delay time.

The function of over-charge detection delay time is same to the discharge over-current detection delay time.

The load short circuit detection delay time are fixed internally.

Fault Detection on DOIT& UVT&OVT

To set the discharge over-current detection delay time, the over-discharge detection delay time and over-charge detection delay time, a capacitor is connected between DOIT/UVT/OVT pin and GND pin.

Take the discharge over-current for example. If the discharge over-current is detected and the DOIT pin is shorted to ground, t_{DOI1} is automatically changed to the DOIT pin short detected 1st discharge over-current detection delay time (t_{DOI1S}).

In the same manner, if the discharge over-current is detected and the DOIT pin is floating, t_{DOI1} is automatically changed to the DOIT pin open detected 1st discharge over-current detection delay time (t_{DOI1O}).

The fault detection function of UVT and OVT are similar to the pin DOIT.

Temperature Protection

JW3312 provides temperature sensing pin TS for detecting the temperature of battery cells. The 103AT NTC (β=3435) resistor is placed nearby battery cells separately. When the temperature of battery pack increases, the voltage of the TS pin decreases. JW3312 detects over-temperature or under-temperature once per t_{DETT} (temperature detection period time). see figure 1 for temperature detection timing chart. In normal status, the JW3312 continuously turns on TB output for t_{EFF_DETT} every t_{DETT}. When the TB output turns on, the external temperature is monitored.

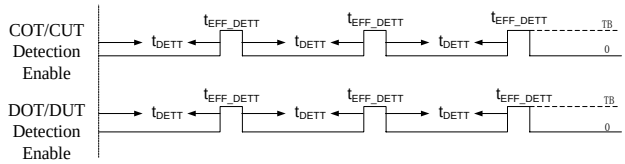


Figure1. Temperature detection timing

During temperature detection, only when VINI>V_{TH_DSG}, the JW3312 considers discharge state. Otherwise, the JW3312 considers charge state.

In charge state, once the battery temperature is beyond V_{COT} or below V_{CUT}, and the state continues for t_{COT_DELAY}, JW3312 shuts down

the charge MOSFET.

The charge temperature protection status is released if either of the following conditions is satisfied.

(1) The temperature of battery pack recovers

(2) The VINI pin voltage is higher than V_{TH_DSG}

In discharge state, once the battery temperature is beyond V_{DOT} or below V_{DUT}, and the state continues for t_{DOT_DELAY}, JW3312 shuts down the discharge MOSFET.

The discharge temperature protection status is released if either of the following conditions is satisfied.

(1) The temperature of battery pack recovers

(2) The VINI pin voltage is lower than V_{TH_CG}

Operation Modes

JW3312 has three power modes: Full Power mode, Sleep mode and Shutdown mode.

For Full Power mode, JW3312 checks for over-voltage, over-discharge, over-temperature, under-temperature every detection period. Besides, over-current events are checked continuously. These safety events decide the status of the charge and discharge MOSFETs. The typical current consumption is 20μA.

JW3312 enters Sleep mode after entering over-discharge status, over-temperature status, under-temperature status or open wire status. The typical current consumption is lower down to be 2μA at sleep mode.

For the other case, JW3312 only waits for temperature events or open wire events releasing.

JW3312 enters Shutdown mode when VDD pin voltage becomes lower than V_{PDOWN}. During this mode, JW3312 does not check for any safety events. The charge and discharge MOSFETs are both off. The typical current consumption is as low as 350nA.

Balance Function

JW3312 provides cells' balance function to balance the cells' capacity in a battery pack. When any cell voltage is higher than Level-1 bleeding threshold voltage V_{BAL1}, and the cell voltage is higher than the lowest cell $\triangle V_{B\_ALLOW}$, the off-chip balance will be turn on and provide about 100mA bleeding current.

Odd-even balance strategy is adopted. The balance period time is 500mS. The first 200mS is used for the odd cells bleeding that satisfy the balance conditions. The second 200mS is used for the even cells bleeding that satisfy the balance conditions. The last 100mS is cell balancing relaxation time before cell voltage measured. See figure 2 for balance operation timing charts.

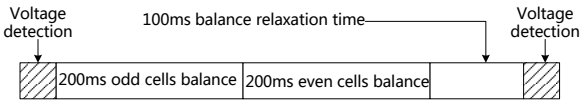


Figure2. Balance operation timing charts

An external resistor of 47Ω recommended should be used to limit the power dissipated by the external MOS. The detailed circuit is shown in the Figure3.

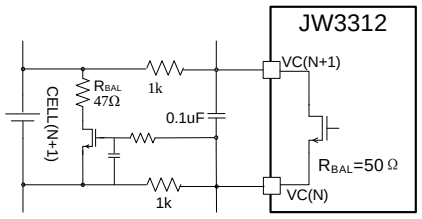


Figure3. External Discharge FET Connection (one cell)

The balance current can be programmable by R_{BAL}.

$$I_{BAL}(\mathrm{A}) = \frac{V_{CELL}(\mathrm{V})}{R_{BAL}(\Omega)} + \frac{V_{CELL}(\mathrm{V})}{1k+1k+R_{BAL}(\Omega)}$$

When the JW3312 is used in extended condition, to avoid the unbalance between IC1 and IC2, the JW3312 provide level-2 balance function. If all the five cell voltage exceed the Level-2 bleeding threshold voltage V_{BAL2}, the external discharge MOS turn on.

The balance exits if one of the conditions mentioned below is satisfied:

(1) When all voltages of VC1, (VC2-VC1), (VC3-VC2), (VC4-VC3) and (VC5-VC4) are lower V_{BAL1}, or higher than VBAL1 and Lower than V_{BAL2}, all the external balance discharge circuits will not work.

(2) When any battery voltage is higher than V_{BAL1}, but lower than the lowest$\triangle V_{B_ALLOW}$

(3) The system entries sleep mode

(4) Open-wire fault is detected.

(5) Battery temperature faults happened.

Open-wire Detection

JW3312 checks for VC5-VC0 open-wire once per detection time period t_{OPEN}.

When any of VC5 to VC0 pin open, it will detect open-wire and charge and discharge is prohibited

The open wire protection is released when open wire point is connected again and the VM pin voltage is lower than V_{VMD}.

3/4/5 cells application selection

When the IC power startup, the TB pin will be short to GND and the TS pin will output current I_{SEL} to R_{SEL}, NTC, 10K before the TB setting up, and the voltage of TS configures the cells number. After cells number configuration, the I_{SEL} will be shutdown. The detailed circuit is shown in the Figure4.

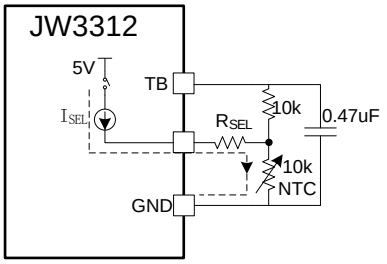


Figure4. 3/4/5 Cells application selection schematic

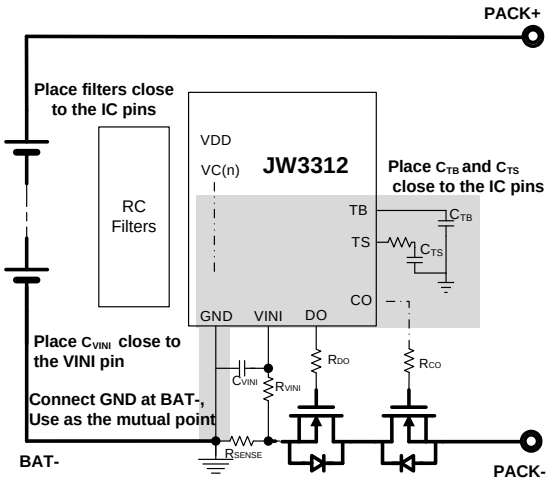
3/4/5 Cells application selection by R_{SEL}

Cells	R_{SEL}	V_{TS}
3	0R	<100mV
4	100k	300mV~600mV
5	300k	>900mV

PCB Layout Precaution

The PCB layout of JW3312 must be carefully designed.

1. The RC filters of VDD and VC(n) should be placed close to the device pins.
2. The capacitors C_{TB} and C_{TS} should be placed near the TB and TS pins.
3. The capacitor C_{VINI} should be placed near the VINI pin
4. The GND should be placed near the R_{SENSE}.



Package and Bag Caution

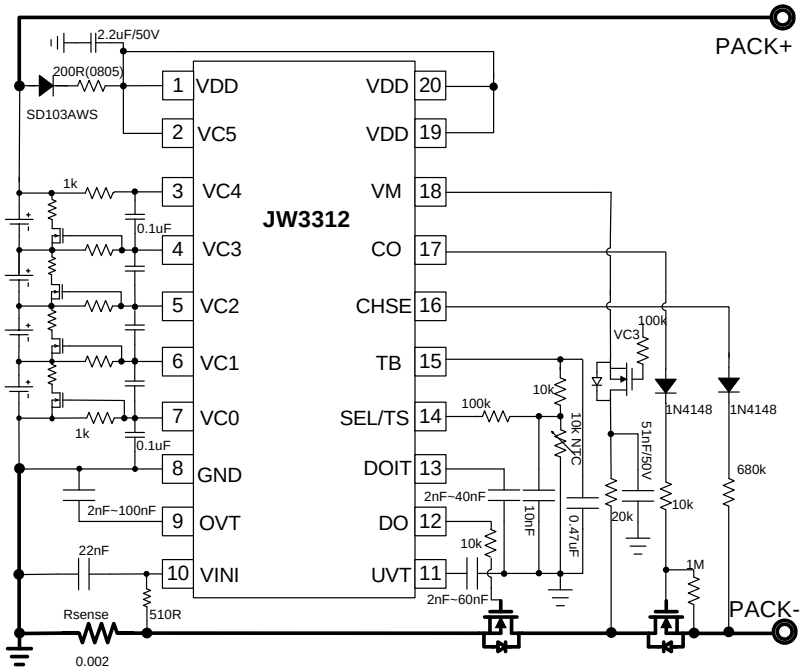
1. JW3312-xxxx is Moisture-Sensitive Devices and its MSL[5)] (Moisture-Sensitive Level) is level-3.
2. Calculated shelf life in sealed bag is 12 months at <40℃ and <90%RH(Relative Humidity).
3. Peak package body temperature[5)] is 260℃.
4. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within 168 hours of factory at the condition ≤30℃/60%RH.
   b) Stored at <10%RH.
5. Devices require bake before mounting if Humidity Indicator Car(HIC) is >10%RH when read at 23±5℃.
6. If baking is required, devices may be baked for 48 hours at 125 ± 5 ℃. If device containers cannot be subjected to high temperature for shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure.

Note:

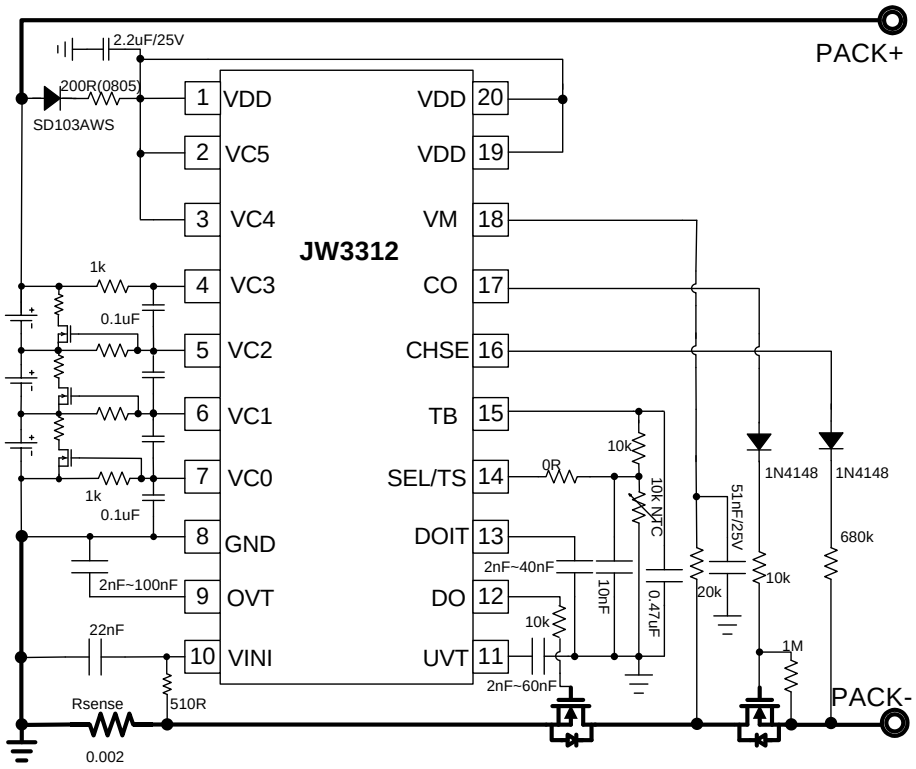
5) Level and body temperature defined by IPC/JEDEC J-STD-020.

REFERENCE DESIGN:

- One PACK- Port (4cells)

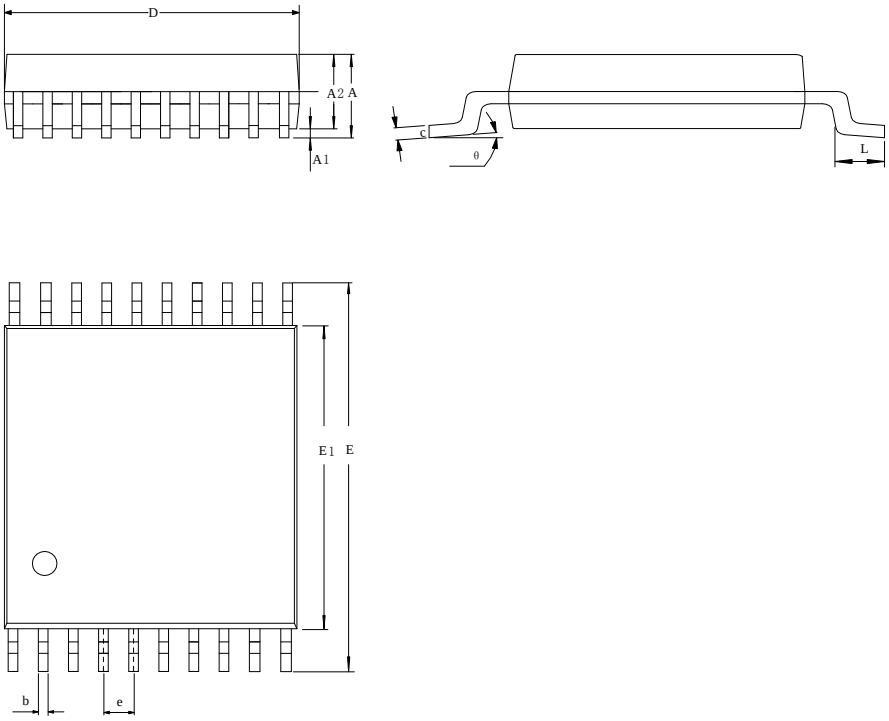


- One PACK- port (3cells)



PACKAGE OUTLINE

TSSOP20 UNIT: mm



Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	0.90	1.00
b	0.19	—	0.30
c	0.09	—	0.20
D	6.40	6.50	6.60
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e	0.65(BSC)		
L	0.50	—	0.70
θ	0°	—	8°

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