JWM9102

6V/2A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®M9102 is a step-down converter module with built-in power MOSFETs and inductor. The JWM9102 is based on COT architecture for fast transient response. Operating with an input range of 2.9V~6V, JWM9102 delivers 2A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in continual conduction mode to maintain low output ripple.

JWM9102 guarantees robustness with output short protection, thermal protection, current run-away protection, and input under voltage lockout.

JWM9102 is available in QFN2.5x3.5x1.6-17 package, which provides a compact solution with minimal external components.

FEATURES

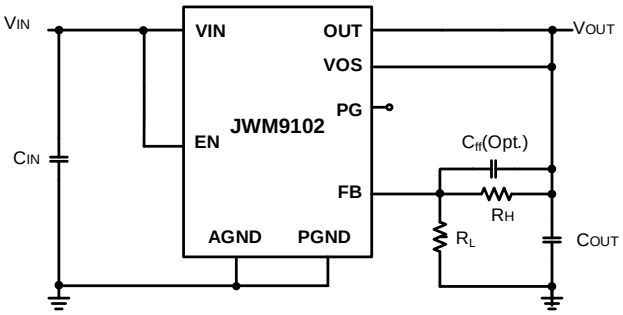
- 2.9V to 6V operating input range
- Up to 2A output current
- Ultra low EMI: pass CISPR22 Class B and CISPR25 Class 5
- 0.6V to V_{IN} adjustable output voltage
- 2MHz switching frequency
- 100% duty cycle for lowest dropout
- Power good indicator
- Output discharge
- Input under voltage lockout
- Output short circuit protection
- Thermal protection
- Available in QFN2.5x3.5x1.6-17 package

APPLICATIONS

- Battery-powered Application
- POL Supply from Li-Ion Battery
- Processor Supplies
- Hard Disk Drives
- Optical Modules
- Medical Instruments
- Portable Devices

TYPICAL APPLICATION

2A Step-down Regulator



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JWM9102QFNAR#TR	QFN2.5x3.5x1.6-17	JWNK□ YW□□□	Green

Notes:

1) JW□□□#TR
- Tape and Reel (If TR is not shown, it means Tube)
- Package Code
- Part No.

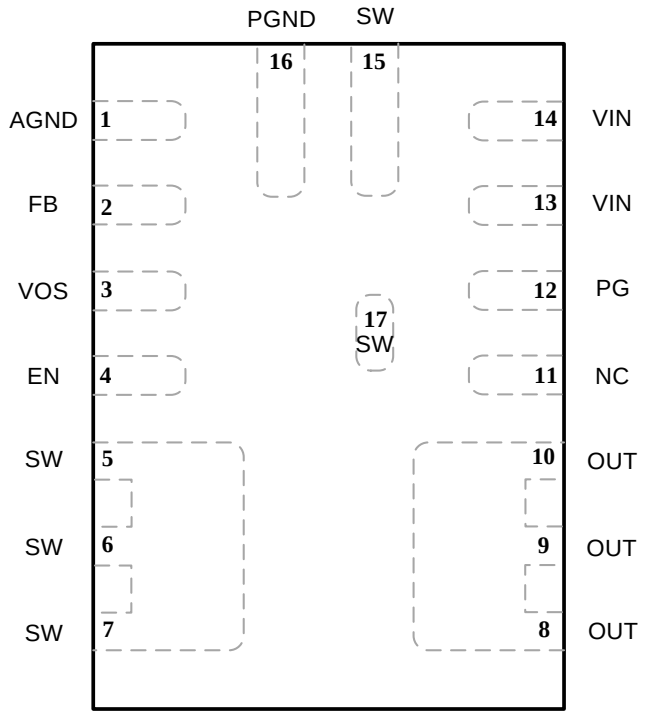
2) Line1: JW □□□
- Product code
- Joulwatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, FB, VOS, PG Pins..... -0.3V to 7V
SW Pin ..... -0.3V(-2.5V for 8ns, -2V for 15ns) to 7V(9V for 10ns, 9.5V for 5ns)
Junction Temperature[2)] 150ºC
Lead Temperature..... 260ºC
Storage Temperature..... -65ºC to +150ºC

ESD RATINGS

Human body model (HBM), per ANSI/ESDA/JEDEC JS-001..... ±2000V
Charged device model (CDM), per JEDEC specification JESD22- V C101..... ±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN} .....2.9V to 6V
Output Voltage V_{OUT} .....0.6V to V_{IN}
Operating Junction Temperature..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
QFN2.5x3.5x1.6-17	50	12ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWM9102 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN=3.6V, T_j=-40℃-125℃，Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	2.7	2.8	2.9	V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		0.1	2	μA
Supply Current	I_Q	V_{EN}=2V, V_{FB}=1.2V		850		μA
Feedback Voltage	V_{FB}	2.9V<V_{IN}<6V	591	600	609	mV
Dropout Resistance[5)]	R_{DR}	100% on duty		56		mΩ
Inductor L Value[5)]	L			0.47		μH
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=6V, V_{EN}=0V, V_{SW}=0V, Tj=25℃			1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=6V, V_{EN}=0V, V_{SW}=6V, Tj=25℃			1	μA
Top Switch Current Limit	I_{LIM_TOP}			3.4	4.2	A
Bottom Switch Current Limit	I_{LIM_BOT}		2	2.7		A
EN High-level Input Threshold Voltage	V_{EN_H}		1.2			V
EN Low-level Input Threshold Voltage	V_{EN_L}				0.4	V
Pull-down Resistance at EN Pin	R_{PD}	EN=Low		400		kΩ
Power Good Threshold Voltage	V_{PG_TH}	Rising	89%	93%	97%	V_{OUT}
		Falling	81%	85%	89%	V_{OUT}
Power Good Output Low	V_{PG_OL}	I_{PG}=-1mA			0.4	V
Soft-Start Time	t_{SS}	Time from EN high to 95% V_{OUT} nominal		1		ms
Output Discharge Resistor	R_{DIS}			200		Ω
Thermal Shutdown[5)]	T_{TSD}			160		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			30		°C
PWM Switching Frequency	F_{SW}	I_{OUT} = 1A		2		MHz

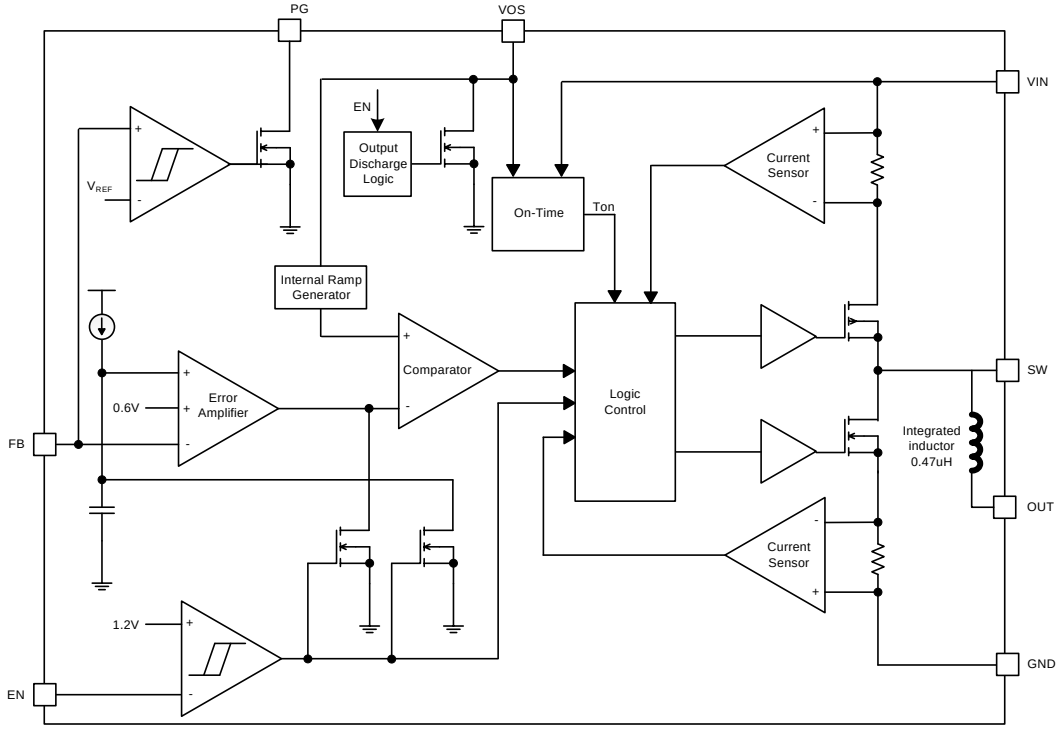
Note：

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	AGND	Analog ground for the internal control circuit.
2	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
3	VOS	Output voltage sense pin and connection for the control loop circuitry.
4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator. This pin has a pull-down resistor of typically 400kΩ.
5 - 7, 15	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
8 - 10	OUT	Power output.
11	NC	No connection.
12	PG	Output power good indicator (High=V_{OUT} ready, Low=V_{OUT} below nominal regulation); open drain (requires pull-up resistor).
13, 14	VIN	Supply voltage for power stage. Connect a 2.9V to 6V supply to V_{IN} and bypass V_{IN} to GND with a suitably large capacitor to eliminate noise on the input to the IC.
16	PGND	Power ground.
17	SW	Do not connect. Leave this pin floating.

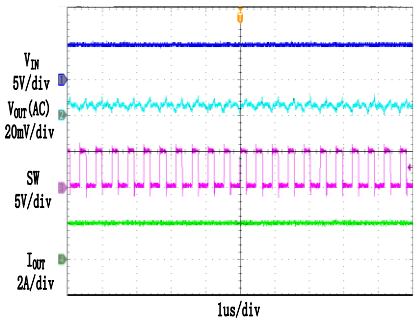
BLOCK DIAGRAM



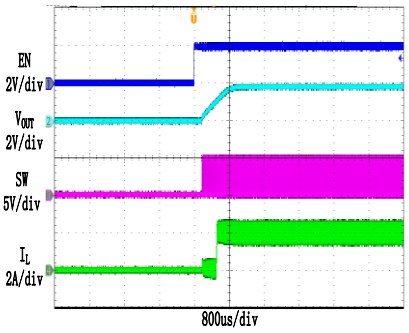
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =5V, V_{OUT} = 1.8V, C_{OUT} = 22µF, TA = +25°C, unless otherwise noted

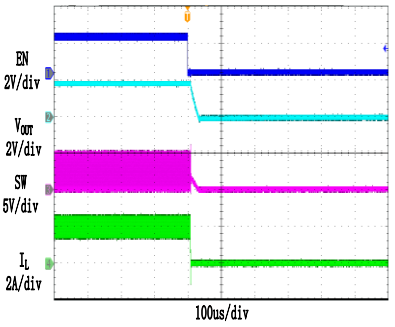
Steady State Test
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=2A



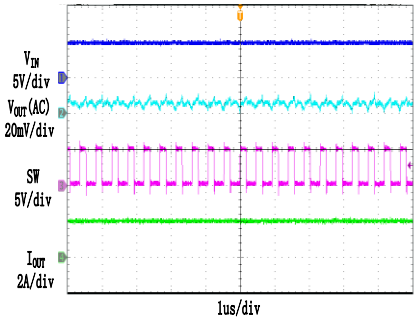
Startup through Enable
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=2A (Eload)



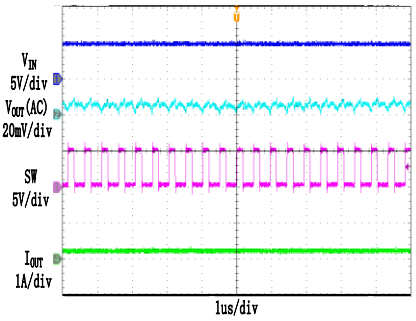
Shutdown through Enable
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=2A (Eload)



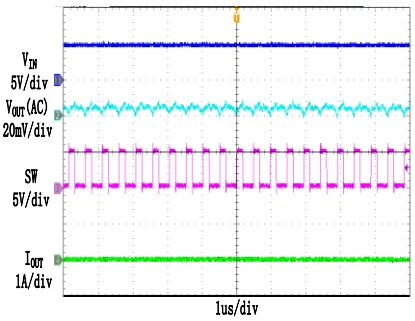
Heavy Load Operation
2A LOAD



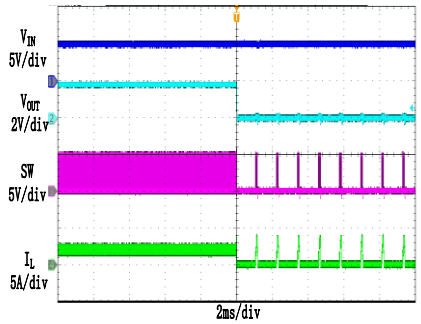
Medium Load Operation
0.2A LOAD



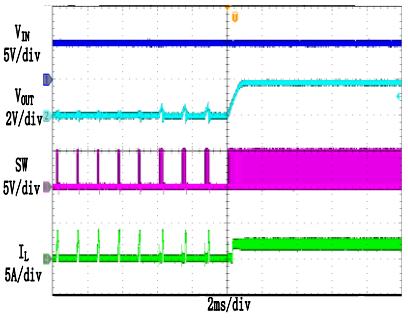
Light Load Operation
0A LOAD



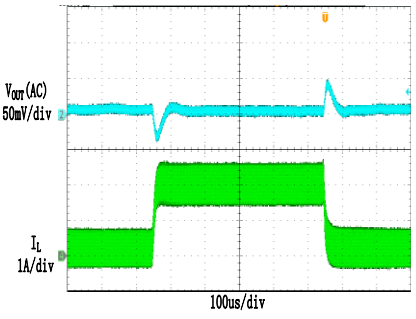
Short Circuit Protection
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=2A - Short



Short Circuit Recovery
V_{IN}=5V, V_{OUT}=1.8V
I_{OUT}=Short-2A



Load Transient
C_{ff}=NC
0.2A LOAD → 2A LOAD → 0.2A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS

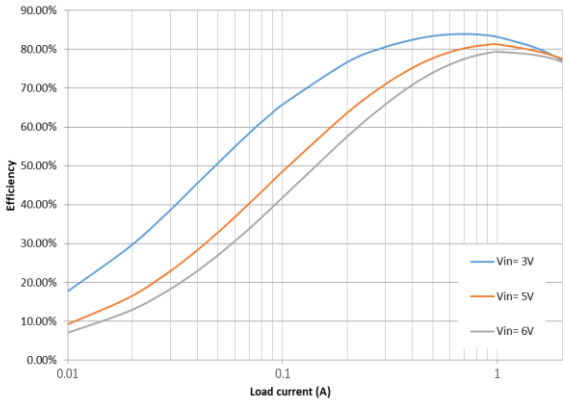


Figure 1. Efficiency vs Load Current (V_{OUT}=0.8V)

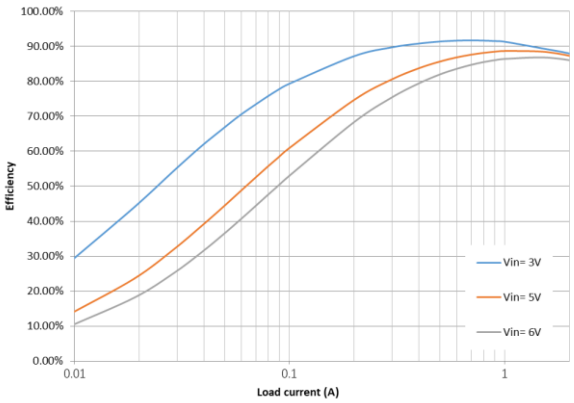


Figure 2. Efficiency vs Load Current (V_{OUT}=1.8V)

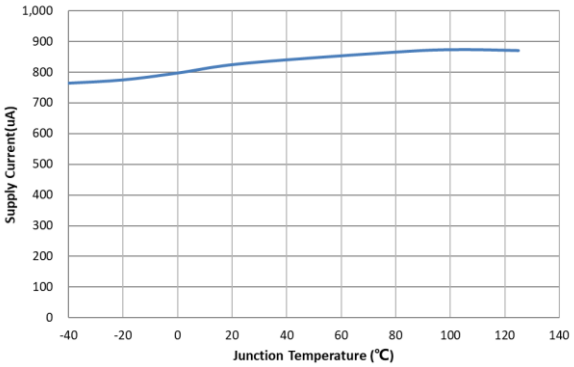


Figure 3. Supply Current vs Junction Temperature

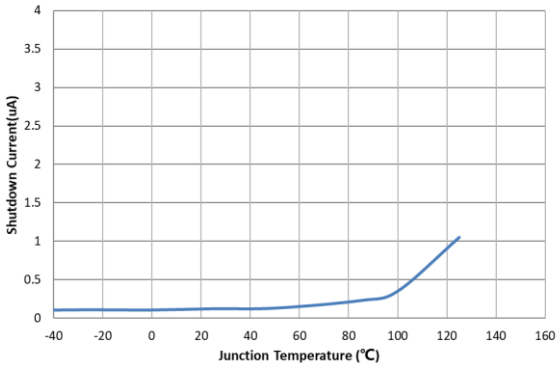


Figure 4. Shutdown Current vs Junction Temperature

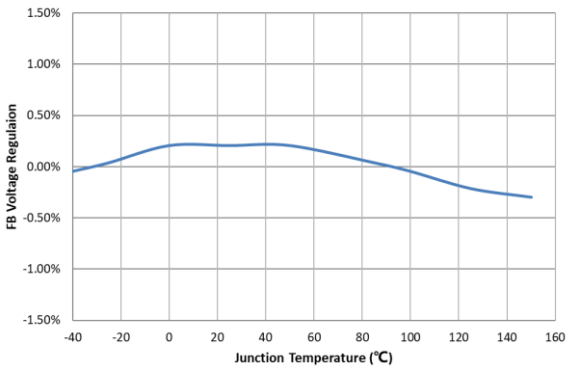


Figure 5. FB Voltage Regulaion vs Junction Temperature

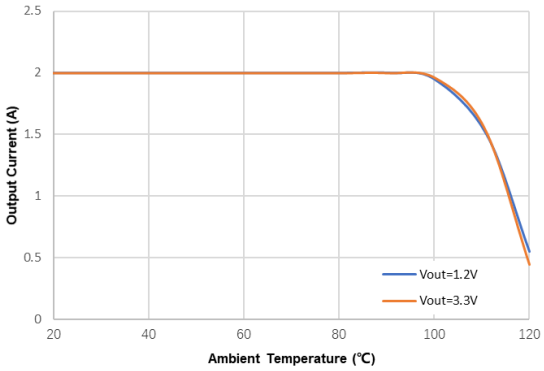
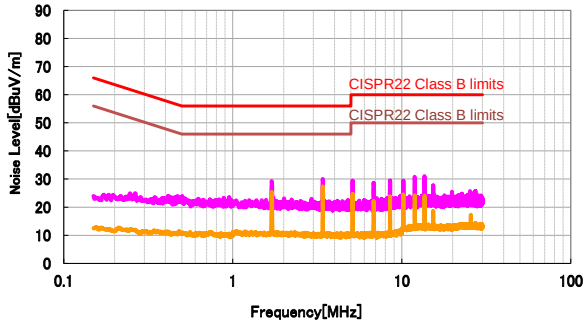


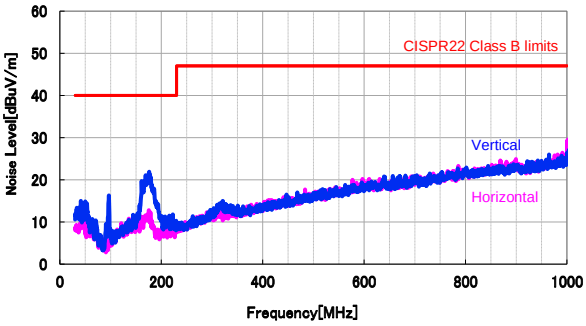
Figure 6. Output current vs. Ambient Temperature, Tj＜125℃

TYPICAL PERFORMANCE CHARACTERISTICS

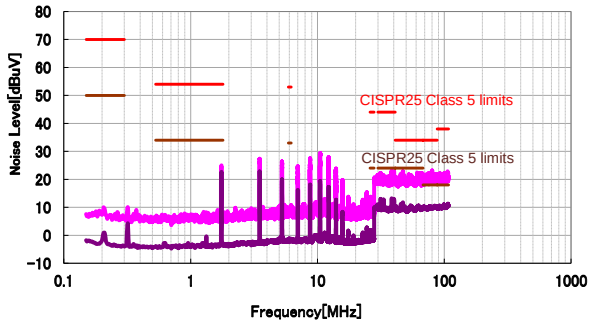
EMI tested on EVM9102



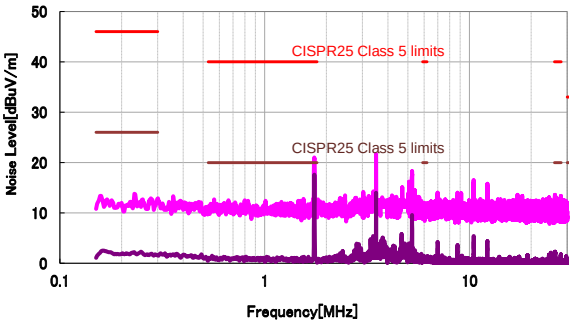
EMI test in CISPR22, Conducted Emission with filter



EMI test in CISPR22, Radiated Emission

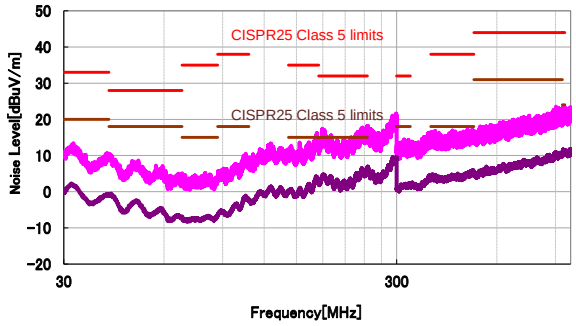


EMI test in CISPR25, Conducted Emission with filter



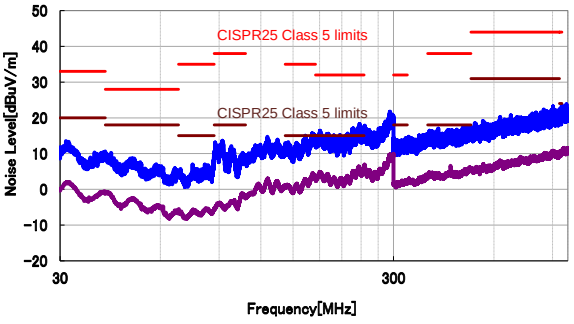
EMI test in CISPR25, Radiated Emission

(150k~30M)



EMI test in CISPR25, Radiated Emission

(30M~1G, Horizontal)



EMI test in CISPR25, Radiated Emission

(30M~1G, Vertical)

FUNCTIONAL DESCRIPTION

The JWM9102 is a constant on-time control, synchronous, step-down regulator. It regulates input voltages from 2.9V~6V down to an output voltage as low as 0.6V, and is capable of supplying up to 2A of load current.

Constant On-time Control

The JWM9102 utilizes constant on-time control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier.

Output of the internal error amplifier is compared with an internal ramp which reflects output voltage ripple to control the on time of the low-side MOSFET.

FCCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps. The JWM9102 is configured to operate in forced CCM (FCCM) operation when the output current is low. In FCCM operation, the switching frequency is fairly constant; hence the output ripple keeps almost the same throughout the whole load range.

Soft-Start and Pre-bias Soft Start

Soft-start is designed in the JWM9102 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source is designed to charge the internal soft-start capacitor and generates a soft-start (SS) voltage. When it is less than internal reference voltage ($V_{REF,}$ typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control. The typical soft start time (from EN high to 95% V_{OUT} nominal) T_{SS} is about 1ms.

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage exceeds the sensed output voltage at FB. This scheme ensures that the converters ramp up smoothly into regulation point.

Shut-Down Mode

The JWM9102 operates in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the JWM9102 drops below 1uA.

Output Voltage Discharge

The JWM9102 enables the output voltage discharge mode. This causes both the high side MOSFET and the low side MOSFET to latch off. A discharge FET connected between SW and GND is turned on to discharges the output VOUT when the Vin pin voltage below the UVLO or the EN pin voltage is below the turn-on threshold. The typical switch on resistance of this FET is about 200Ω.

Power Switches

P-channel and N-channel MOSFET switches are integrated on the JWM9102 to down convert the input voltage to the regulated output voltage.

100% Duty Cycle Low Dropout Operation

The devices offer low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. This is particularly useful in battery powered applications to achieve the

longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain output regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times R_{DR}$$

Where

V_{IN_MIN} is the minimum input voltage to maintain an output voltage;

I_{OUT_MAX} is the maximum output current;

R_{DR} is the high-side MOSFET on-resistance and the inductor conductive resistance in series.

Current Limit and SCP

JWM9102 have protection against heavy load and short circuit events which switch current limits are designed in JWM9102. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM_TOP}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Only when output current drops below the valley current limit I_{LIM_BOT} can the top power switch be turned on again. When this switch current limit is triggered 32 times, the devices stop switching and enable the output discharge. The devices then automatically start anew start-up after a typical delay time of 66μs has passed. The devices repeat this mode until the high load condition is removed.

Power Good

JWM9102 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing for multiple rails. The PG pin is an open drain output. It can sink 1mA of current and maintain its specified logic low level. JWM9102 features PG=Low when the device is turned-off due to EN or thermal shutdown. When the device is in UVLO, the PG pin is in high resistance state.

Thermal Protection

When the core temperature of the JWM9102 rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C, the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_L}{R_L + R_H}$$

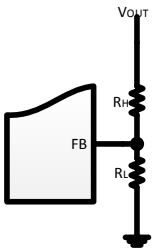
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_L around 10kΩ, and then R_H can be calculated by:

$$R_H = R_L \cdot \left(\frac{V_{OUT}}{0.6} - 1 \right)$$

The following table lists the recommended values.

V_{OUT} (V)	R_L(kΩ)	R_H(kΩ)
1	30	20
1.2	20	20
1.8	10	20
3.3	11	49.9



Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{CIN} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_{IN} is the input capacitance value, fs is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 10uF/0805/10V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot fs \cdot C_{OUT}} \right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

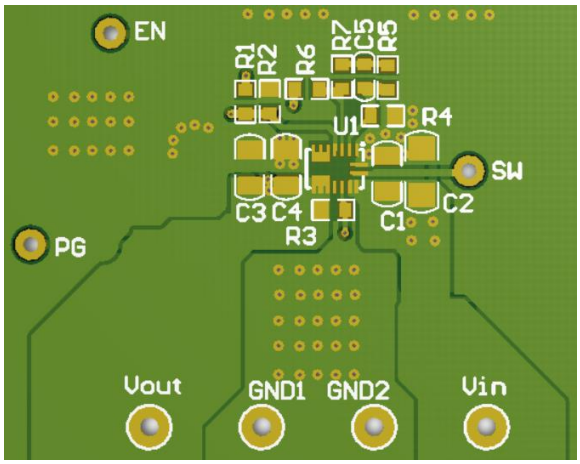
The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and 44μF ceramic capacitors are recommended in typical application.

PCB Layout Note

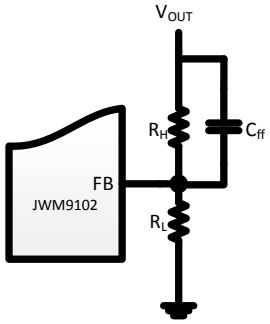
For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JWM9102 (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling.
5. Make VIN, VOUT and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
6. The traces should not be routed under PIN 17 to eliminate the noise.



External Components Suggestion:

V_{OUT} (V)	R_L (kΩ)	R_H (kΩ)	C_{ff} (pF)	C_{OUT} (μF)
1	30	20	NC	44~66
1.2	20	20	NC	22~44
1.8	10	20	NC	22~44
3.3	11	49.9	NC	22~44



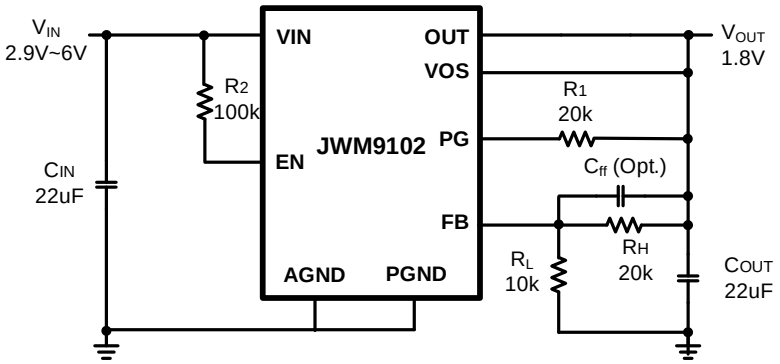
REFERENCE DESIGN

Reference 1:

V_{IN} : 2.9V~6V

V_{OUT} : 1.8V

I_{OUT} : 0~3A

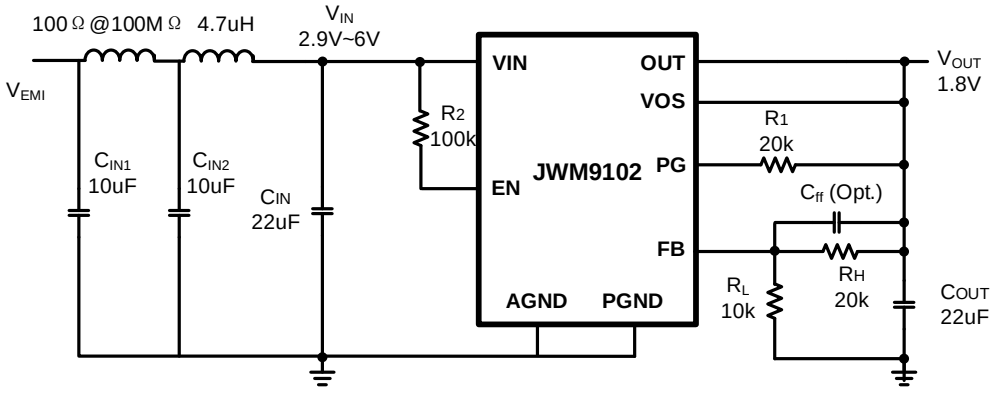


Reference 2 (EMI Test Circuits):

V_{IN} : 2.9V~6V

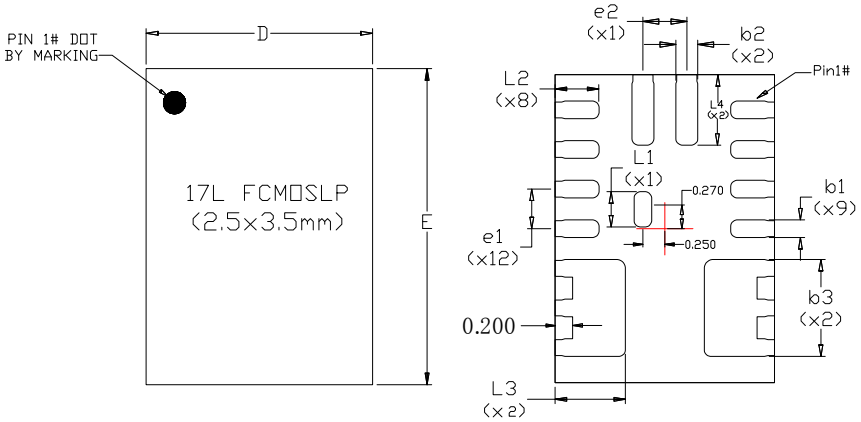
V_{OUT} : 1.8V

I_{OUT} : 0~3A

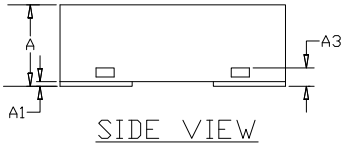


PACKAGE OUTLINE

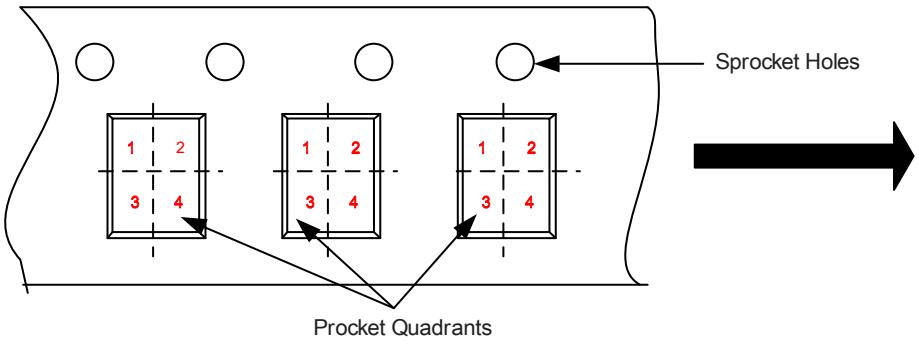
QFN2.5x3.5x1.6-17 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.55	1.60	1.65
A1	—	—	0.05
A3		0.203 REF	
b1	0.15	0.20	0.25
b2	0.20	0.25	0.30
b3	1.05	1.10	1.15
D	2.45	2.50	2.55
E	3.45	3.50	3.55
e1		0.45 BSC	
e2		0.50 BSC	
L1	0.35	0.40	0.45
L2	0.45	0.50	0.55
L3	0.75	0.80	0.85
L4	0.75	0.80	0.85



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN2.5x3.5x1.6-17	1

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