JWH5085

16V/12A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H5085 is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 2.7V~16V, JWH5085 delivers 12A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. The operation frequency is set easily to 600 kHz, 800 kHz, or 1000 kHz with the MODE configuration, allowing the JWH5085 frequency to remain constant regardless of the input/output voltages. JWH5085 guarantees robustness with output short protection, over-voltage protection, thermal protection and under voltage protection.

JWH5085 is available in QFN3×4-21 package, which provide a compact solution with minimal external components.

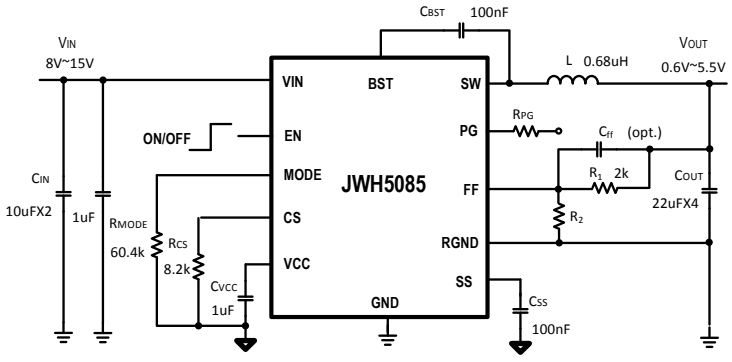
FEATURES

- 2.7V to 16V operating input range with external 3.3V VCC bias
- 4V to 16V operating input range with internal bias or external 3.3V VCC bias
- 12A output current
- Differential output voltage remote sense
- Programmable accurate current limit level
- ±0.5% reference voltage over 0℃ to +70℃ junction temperature range
- Selectable PFM or FCCM
- Power good indicator
- Programmable soft-start time
- Selectable switching frequency from 600kHz, 800kHz, and 1000kHz
- Output discharge function
- Non-latch OCP, UVP, OVP, UVLO Thermal protection
- Available in QFN3X4-21 package

APPLICATIONS

- Telecom and Networking Systems
- Server, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load

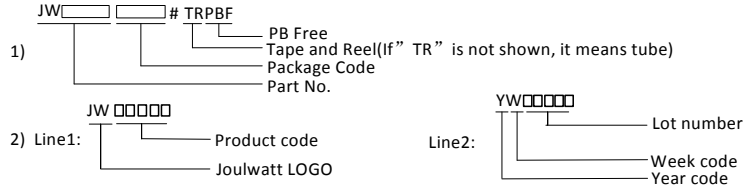
TYPICAL APPLICATION



ORDER INFORMATION

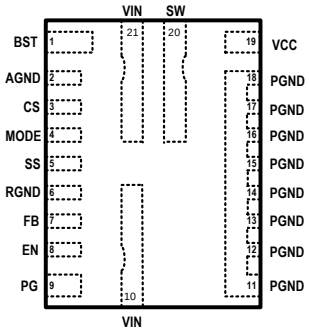
DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JWH5085QFNAG#TRPBF	QFN3X4-21	JWH5085 YW□□□□□

Notes:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

VIN Pin..... -0.3V to 18V
SW Pin..... -0.3V (-5V for 25ns) to 18V (25V for 25ns)
BST Pin..... SW-0.3V to SW+4V
VCC Pin ..... -0.3V to 4V
All Other Pins..... -0.3V to 4V
Junction Temperature[2)] 150ºC
Lead Temperature..... 260ºC
Storage Temperature.....-65 ºC to +150 ºC
ESD Susceptibility (Human Body Model) ..... ±2kV
Charged device model (CDM), per JEDEC specification JESD22- V C101..... ±500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN} .....4V to 16V
Output Voltage V_{OUT} ..... 0.6V to 5.5V
External VCC Bias V_{CC_EXT} ..... 3.16V to 3.6V
Maximum Output Current I_{OUT_MAX} 12A
Maximum Output Current Limit I_{OC_MAX} 16A
Maximum Peak Indutcor Current Limit I_{L_Peak} 18A
Operation Junction Temperature T_j.. ..... -40°C to 125°C

THERMAL PERFORMANCE[4)]

	θ_{JB} [5)]	θ_{Jc_TOP} [5)]
QFN3X4-21	9	21ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH5085 include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB.

5) θ_{JB} Thermal resistance from junction to board around PGND pin soldering point.

θ_{Jc_TOP} Thermal resistance from junction to top of package.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C ~125°C, unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_HTH}	V_{IN} rising, V_{CC}=3.3V		2.4		V
	V_{IN_LTH}	V_{IN} falling, V_{CC}=3.3V		1.85		V
Shutdown Current	I_{SD}	EN=0		0.5		μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=0.7V		550		μA
Enable Input Rising Threshold	V_{EN_HTH}			1.22		V
Enable Hysteresis	$V_{EN\_TH\_HYS}$			200		mV
Feedback Voltage	V_{REF}	T_J= 0°C to 70°C		600		mV
		T_J= -40°C to 125°C		600		mV
Top Switch Resistance	$R_{DS(ON)T}$			13.3		mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			4.3		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=16V, V_{SW}=0V			10	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=16V, V_{SW}=16V			10	μA
Current Limit Threshold	V_{LIM}			1.2		V
ICS to IOUT ratio	I_{CS}/I_{OUT}	I_{OUT} ≥2A		20		μA/A
Bottom Switch Negative Current Limit	I_{LIM_NEG}			-13		A
Minimum On Time[6)]	T_{ON_MIN}			50		ns
Minimum Off Time	T_{OFF_MIN}			100		ns
Switching Frequency[7)]	F_{SW}	MODE=GND		600		kHz
		MODE=30.1K		800		kHz
		MODE=60.4K		1000		kHz
Discharge FET Ron	R_{DIS}			80		Ω
Soft-Start Charge Current	I_{SS_CHAR}	V_{SS}=0V		42		μA
Soft-Start Discharge FET Ron	$R_{SS\_DISCHAR}$	V_{CC}=3V		1.5		kΩ
Soft-Start Time[6)]	T_{SS}	C_{SS}=1nF		1		ms
VCC Under-voltage Lockout Threshold	V_{CC_HTH}	VCC rising		2.8		V
	V_{CC_LTH}	VCC falling		2.5		V
VCC Regulator	V_{CC}			3.0		V
VCC Load Regulation		I_{CC}=25mA		0.5		%
Power Good High Threshold	PG_{HTH}	FB from low to high		92.5%		V_{REF}
		FB from high to low		105%		V_{REF}
Power Good Low Threshold	PG_{LTH}	FB from low to high		116%		V_{REF}
		FB from high to low		80%		V_{REF}

V_{IN}=12V, T_J=-40°C ~125°C, unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Power Good Delay Time	$PG_{\_DLY}$	PG from low to high		0.9		ms
Power Good Sink Current	I_{PG}	PG=0.5V	10			mA
Power Good Low-level Output Voltage	V_{OL_100}	V_{IN}=0V, Pull PG up to 3.3V through a 100kΩ resistor		650		mV
	V_{OL_10}	V_{IN}=0V, Pull PG up to 3.3V through a 10kΩ resistor		750		mV
Output Over-voltage Threshold		V_{FB} Rising		116%		V_{SET}
Output Under-voltage Threshold[6)]		V_{FB} Falling		80%		V_{SET}
Thermal Shutdown[6)]	T_{TSD}			160		°C
Thermal Shutdown Hysteresis[6)]	T_{TSD_HYST}			30		°C

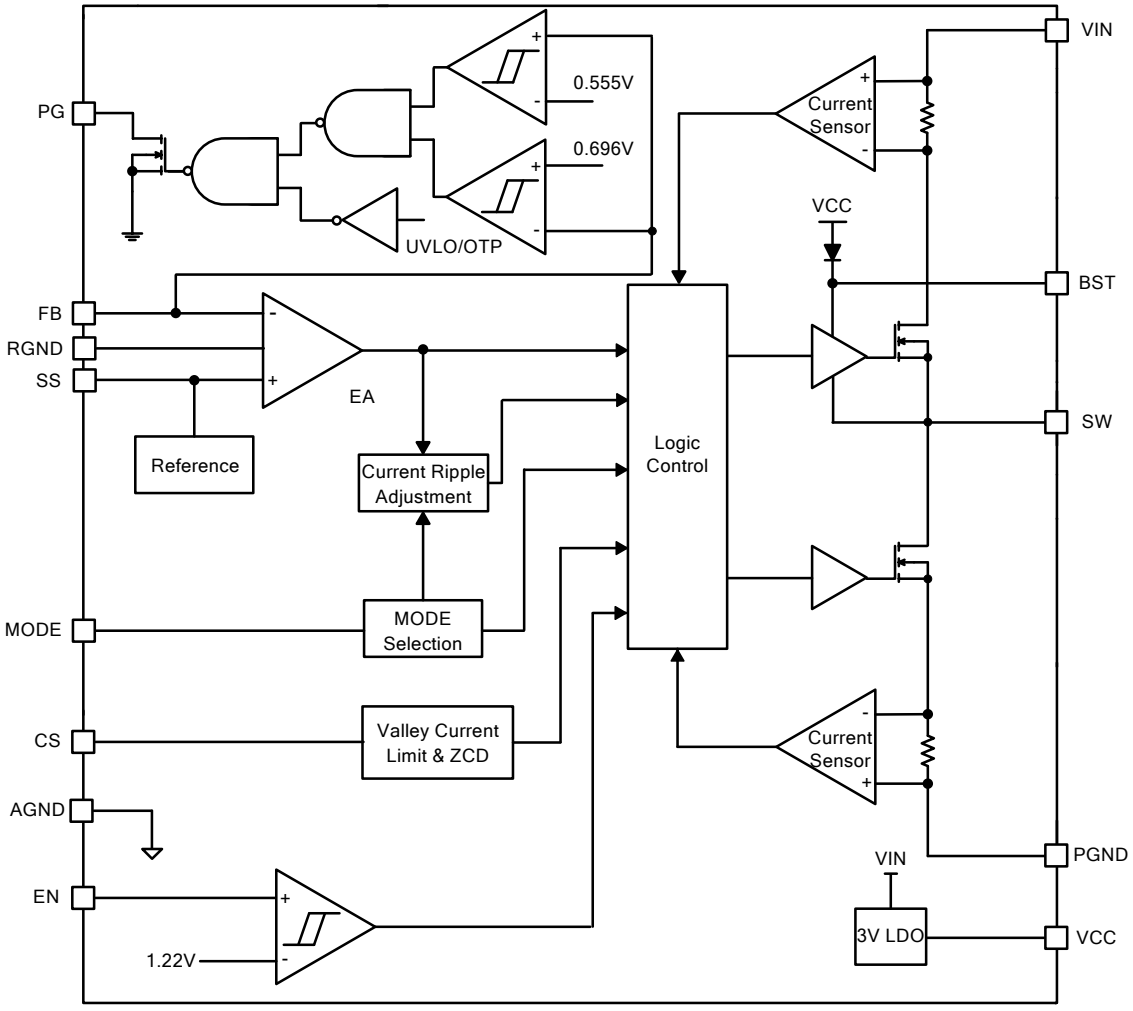
Note:

6) Guaranteed by design.
7) Guaranteed by design over all temperature range

PIN DESCRIPTION

Pin	Name	Description
1	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
2	AGND	Analog ground pin. Select AGND as the control circuit reference point.
3	CS	Current limit. Connect a resistor to AGND to set the current limit trip point.
4	MODE	Operation mode selection. Program MODE to select CCM, pulse skip mode, and the operating switching frequency.
5	SS	Soft-start time setting pin. The soft-start time is determined by the capacitance between SS pin and AGND.
6	RGND	Differential remote sense negative input. Connect this pin directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
7	FB	Feedback (Differential remote sense positive input). An external resistor divider from the output to RGND (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	Enable control pin. Pull this pin high to turn on the regulator. Do not leave this pin floating.
9	PG	Power good monitor output. Open drain output when the output voltage is within 92.5% to 116% of internal reference voltage.
10, 21	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4V to 16V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
11-18	GND	Power ground pin
19	VCC	Internal 3V LDO Output. Power supply for internal analog circuits and driving circuit. Decouple this pin to ground with a minimum 1uF ceramic capacitor.
20	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JWH5085 is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 2.7V to 16V down to as low as 0.6V output voltage, and is capable of supplying up to 12A of load current.

Power Switch

N-Channel MOSFET switches are integrated on the JWH5085 to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal/external 3V rail when SW is low.

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps. The JWH5085 can also be configured to operate in forced CCM operation when the output current is low (See ***Mode Selection*** section for details). In CCM operation, the switching frequency is fairly constant; hence the output ripple keeps almost the same throughout the whole load range.

PFM Operation

At light load condition, the JWH5085 can be configured to work in PFM mode to optimize the efficiency. When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to PFM mode if the JWH5085 is configured so (see ***Mode Selection*** section for details).

In PFM mode operation, the high side MOSFET is turned off by the peak current reference and the low side MOSFET turns on until the inductor current reaches zero. At this time, the output voltage is still higher than the target value which causes the internal COMP voltage lower than a clamp value, and the high side MOSFET is not allowed to turn on until the COMP voltage rises above its clamp voltage.

At light load condition, the high side MOSFET is not turned on as frequently in PFM mode as it is in forced CCM. As a result, the efficiency in pulse skip mode is improved greatly, comparing with that in forced CCM operation.

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The high side MOSFET is turned on more frequently. Hence, the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with the following equation:

$$I_{OUT} := \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{2 \cdot L \cdot f_{SW} \cdot V_{IN}}$$

The part enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Mode Selection

The JWH5085 provides both forced CCM operation and PFM mode operation in a light-load condition. The JWH5085 has three options for switching frequency selection.

Selecting the operation mode under light load condition and the switching frequency is done

by choosing the resistance value of the resistor connected between MODE and AGND or VCC (See Table 1).

Table 1 --- MODE selection

MODE	Light-load Mode	Switching Frequency
VCC	PFM	600kHz
243kΩ(±20%) to GND	PFM	800kHz
121kΩ(±20%) to GND	PFM	1000kHz
GND	FCCM	600kHz
30.1kΩ(±20%) to GND	FCCM	800kHz
60.4kΩ(±20%) to GND	FCCM	1000kHz

Shut-Down Mode

The JWH5085 shuts down when voltage at EN pin is below 0.3V. The entire regulator is off and the supply current consumed by the JWH5085 drops below 5uA.

VIN Under-Voltage Protection

In addition to the enable function, the JWH5085 provides an Under Voltage Lock-out (UVLO) function that monitors the input voltage. To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when input voltage drops below the UVLO-falling threshold. The IC resumes switching when input voltage exceeds the UVLO-rising threshold.

Enable and Adjustable UVLO Protection

The JWH5085 is enabled when the VIN pin voltage rises above 2.4V and the EN pin voltage exceeds the enable threshold of 1.22V. The JWH5085 is disabled when the VIN pin voltage falls below 1.85V or when the EN pin voltage is below 1.02V. Do not leave this pin floating.

If an application requires a higher VIN under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 1). So that when VIN rises to the pre-set value, EN rises above 1.22V to enable the device and when VIN drops below the pre-set value, EN drops below 1.02V to trigger input under voltage lockout protection.

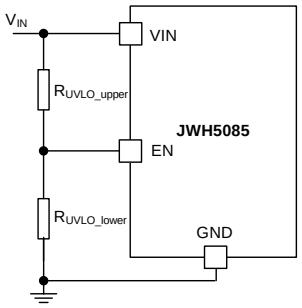


Fig. 1 Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$V_{UVLO} := \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \cdot V_{EN\_TH}$$

$$V_{UVLO\_HYS} := \frac{R_{UVLO\_upper} + R_{UVLO\_lower}}{R_{UVLO\_lower}} \cdot V_{EN\_HYS}$$

where

V_{EN_TH} is enable shutdown threshold (1.22V typ.);

V_{EN_HYS} is enable shutdown hysteresis (200mV typ.).

Soft Start

Soft-start is designed in JWH5085 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 42uA is designed to charge the external soft-start capacitor (C_{SS}) and generates a soft-start (SS) voltage ramping

up from 0V to 1.5V. When it is less than internal reference voltage ($V_{REF,}$ typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

The soft start time (10% to 90%) T_{SS} can be calculated by the following equation.

$$T_{SS}(ms) := \frac{C_{SS}(nF) \cdot V_{REF}(V) \cdot 0.8}{I_{SS}(\mu A)}$$

where C_{SS} is the soft-start capacitance connected between SS pin and AGND pin.

At power up, the soft start pin is discharged before MOSFETs switching to ensure a proper power up. Also, during normal operation, the JWH5085 will stop switching and the soft-start pin will be discharged, when the VIN UVLO is exceeded, EN pin pulled below 1.02V, or a thermal shutdown event occurs.

Current Sense and Over-Current Protection (OCP)

The JWH5085 features an on-die current sense and a programmable positive current limit threshold.

The current limit is active when the JWH5085 is enabled. During the low side MOSFET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The high side MOSFET is only allowed to turn on when the V_{CS} voltage is below the internal OCP voltage threshold V_{OCP} (during the low side MOSFET on state) to limit the SW valley current cycle-by-cycle.

The following equation calculates the current limit threshold setting from R_{CS}:

$$R_{CS}(\Omega) := \frac{V_{OCP}}{G_{CS} \cdot \left[I_{LIM} - \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \cdot \frac{1}{2 \cdot L \cdot f_{SW}} \right]}$$

where

V_{OCP}=1.2V,

G_{CS} = 20 μA/A, and

I_{LIM} = the desired output current limit.

The OCP HICCUP is active 3ms after the JWH5085 is enabled, Once OCP HICCUP is active, if the JWH5085 detects over-current condition for consecutive 31 cycles, or if the FB drops below under-voltage protection (UVP) threshold, it enters HICCUP mode. In HICCUP mode, the JWH5085 latches off the high side MOSFET immediately, and latches off low side MOSFET after ZCD is detected. Meanwhile, the SS capacitor is also discharged. After about 11ms, the JWH5085 will try to soft start automatically. If the over-current condition still holds after 3ms of running, the JWH5085 repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Negative Inductor Current limit

When the low side MOSFET detects a -13A current, the part turns off the low side MOSFET to limit the negative current.

Output Sinking Mode (OSM)

The JWH5085 employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When the FB voltage is higher than 104%*V_{REF} but is below the OVP threshold, it triggers OSM. During OSM operation, the low side MOSFET remains on until it hits the -13A negative current limit. Upon hitting -13A, the low side MOSFET is momentarily turned off and is then turned on again when the negative current reaches to zero. The JWH5085 keeps this operation until the FB drops below 102%*V_{REF}.

Pre-Bias Start-Up

The JWH5085 has been designed for a

monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side MOSFETs until the voltage on the SS capacitor exceeds the sensed output voltage at FB. Before SS voltage reaches pre-biased FB level, if the BST voltage (from BST to SW) is lower than 1.8V, the low-side MOSFET is turned on to allow the BST voltage to be charged through VCC. The low-side MOSFET is turned on for very narrow pulses, so the drop in pre-biased level is negligible.

Output Voltage Discharge

When the JWH5085 is disabled through EN, it enables the output voltage discharge mode. This causes both the high side MOSFET and the low side MOSFET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 10%* V_{REF}, the discharge FET is turned off.

Output Over-voltage Protection

The JWH5085 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an overvoltage condition. This provides auto-recovery OVP mode.

If the FB voltage exceeds 116% of the REF voltage, it enters OVP mode. The high side MOSFET is turned off and PGOOD goes low until the FB voltage drops below 105% of REF voltage. Meanwhile, the low side MOSFET remains on until it hits the low-side negative current limit (NOCP). Once it hits NOCP, the low side MOSFET is turned off and the high side MOSFET is turned on until the negative current reaches to zero. If the FB voltage is still higher than 102% of REF voltage, the low side MOSFET is then turned on again. The JWH5085 keeps this operation to try to bring down the output voltage. When the FB voltage drops below 102% of the REF voltage, the low side MOSFET is turned off for PFM operation, and keeps turning on for FCCM operation. If FB rises back to more than 116% of the REF voltage, the low side MOSFET turns off again with NOCP until FB drops back below 102% of the REF voltage.

Power Good

The JWH5085 has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to VCC or another voltage source through a resistor. After applying the input voltage, the MOSFET turns on, so PG is pulled to GND before SS is ready. After the FB voltage reaches 92.5% of the REF voltage, PG is pulled high after a 0.9ms delay.

When the FB voltage drops to 80% of the REF voltage, PG is pulled low within 1us deglitch time. When the FB voltage rises above 92.5% of the REF voltage, PG is pulled high again after a 0.9ms delay time.

When the FB voltage exceeds 116% of the REF voltage, PG is pulled low within 1us deglitch time. When the FB voltage drops to 105% of the REF voltage, PG is pulled high again with 0.9ms deglitch time.

Once EN UVLO or OTP is triggered, PG is pulled low within 1us deglitch time even FB voltage is still in threshold range.

If the input supply fails to power the JWH5085, PG is clamped low even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 2 below:

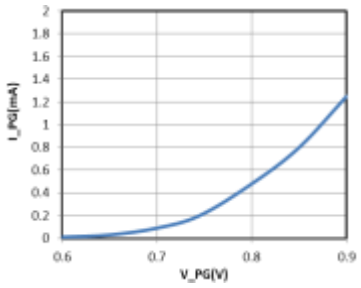


Fig. 2 Power Good clamped voltage vs. pull-up current

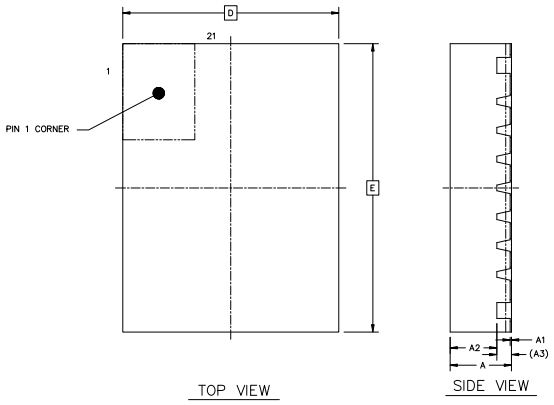
Thermal Protection

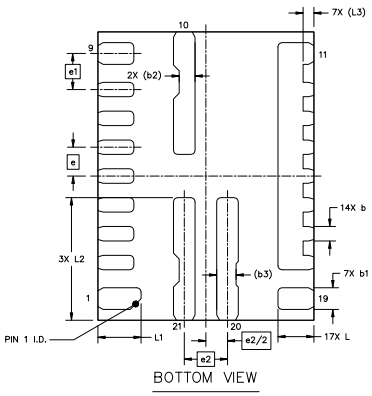
When the temperature of the JWH5085 rises above 160°C, it is forced into thermal shut-down.

Only when core temperature drops below 130°C can the regulator becomes active again.

PACKAGE OUTLINE

QFN3X4-21 UNIT: mm





SYMBOL	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.02	0.05
A2	---	0.65	---
A3		0.203 REF	
b	0.15	0.2	0.25
b1	0.25	0.3	0.35
b2		0.22 REF	
b3		0.27 REF	
D		3 BSC	
E		4 BSC	
e		0.4 BSC	
e1		0.5 BSC	
e2		0.6 BSC	
L	0.4	0.5	0.6
L1	0.5	0.6	0.7
L2	1.6	1.7	1.8
L3		0.15 REF	

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