JWH3530

Active Clamp PWM Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®H3530 is a highly integrated dual−mode active−clamp PWM controller targeting next−generation high−density, high−performance and small to medium power level isolated dc−dc converters for use in telecom and datacom industries. It can be configured in either voltage mode control with input voltage feed−forward or peak current mode control. Peak current mode control may be implemented with input voltage feedforward as well. Adjustable adaptive overlap time optimizes system efficiency based on input voltage and load conditions.

This controller integrates all the necessary control and protection functions to implement an isolated active clamp forward or asymmetric half−bridge converter. It integrates a high−voltage startup bias regulator. The JWH3530 has a line under voltage detector, cycle−by−cycle current limiting, line voltage dependent maximum duty ratio limit, over voltage protection, and programmable over temperature protection using an external thermistor. It also includes a dual−function FLT/SD pin used for communicating the presence of a fault but also for shutting down the controller. A dedicated dual−function synchronization pin eases operations when associating bricks together.

FEATURES

- Support Voltage Mode Control and Peak Current Mode Control
- Adaptive Overlap Time Control for Improved Efficiency
- Integrated 120−V High Voltage Startup Circuit with Self−Supply Operation
- Programmable Maximum Duty Ratio Clamp
- Programmable Soft−Start
- Programmable Oscillator with a 1 MHz Maximum Frequency and Synchronization Capability
- Main Switch Drive Capability of −2A / 3A
- Active Clamp Switch Drive Capability of −2A /1 A
- Line Under Voltage Lockout (UVLO) with Adjustable Hysteresis
- Cycle by Cycle Peak Current Limiting
- Adjustable Over Power Protection
- OCP / SCP / External OTP / Over Voltage Protection through a Dedicated Pin
- FLT/SD Pin Used for Fault Reporting and Shutdown Input
- QFN24 Package

APPLICATIONS

- Server Power Supplies
- High−Efficiency Isolated Dc−Dc Converters
- 24V and 48 V Telecom Systems
- 42 V Automotive Applications

TYPICAL APPLICATION

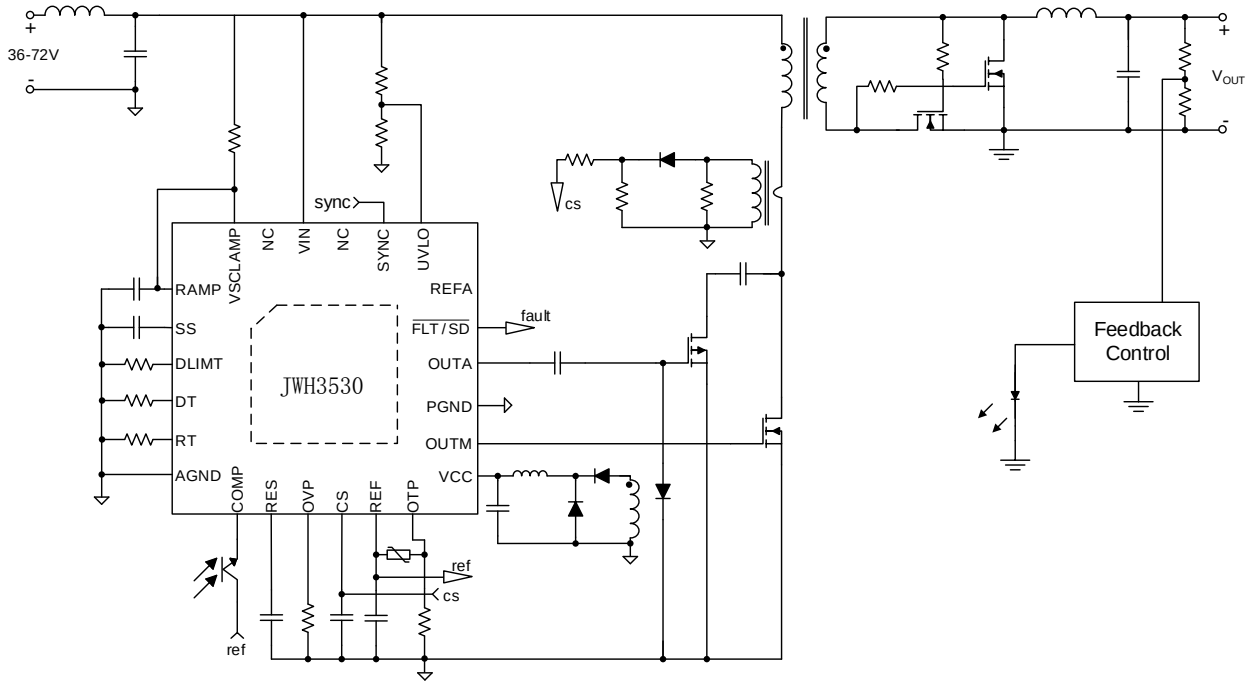


Figure 1.Typical application circuit with voltage mode control

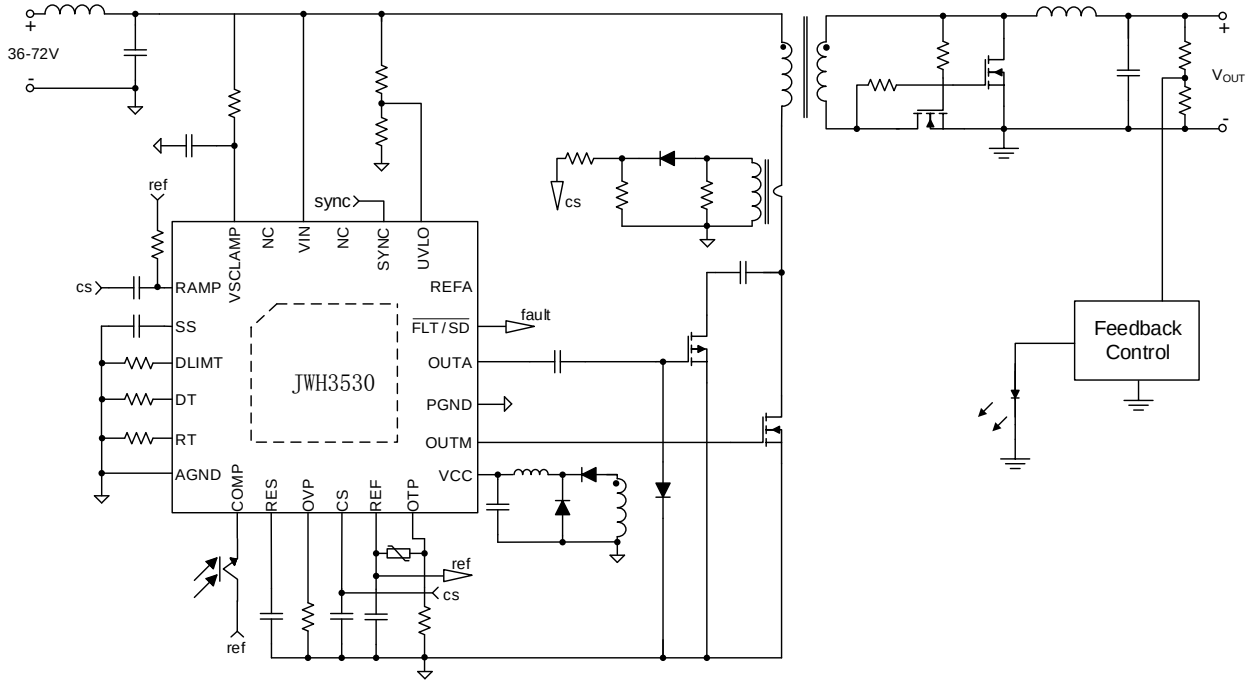
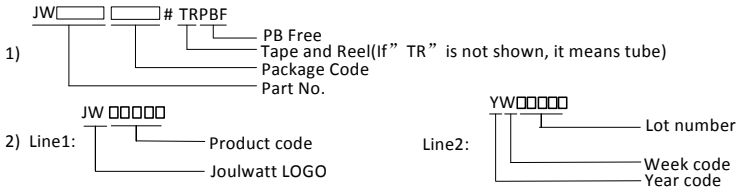


Figure 2. Typical application circuit with current mode control

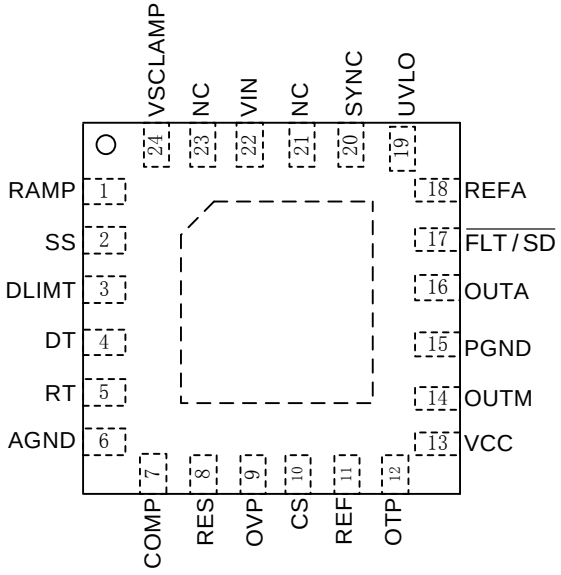
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JWH3530QFND#TRPBF	QFN4X4-24	JWH3530 YW□□□□□

Notes:



PIN CONFIGURATION



QFN24 (Top View)

ABSOLUTE MAXIMUM RATING[1)]

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage – Continuous operation	V_{IN}	-0.3 to 120	V
Supply Input Voltage	$V_{CC(MAX)}$	-0.3 to 20	V
UVLO Input Voltage	V_{UVLO}	-0.3 to V_{CC}	V
Main/Active Clamp Driver Maximum Voltage	V_{OUTM}/V_{OUTA}	-0.3 to V_{CC}	V
COMP Input Voltage	V_{COMP}	-0.3 to 5.5	V
All Other Pins Voltage Range		-0.3 to 7	V
Operating Junction Temperature	T_J	-40 to 150	ºC
Storage Temperature	T_{stg}	-60 to 150	ºC
ESD Capability (Human Body Model)		>2000	V
ESD Capability (Charge Device Model)		>1500	V

RECOMMENDED OPERATING CONDITIONS

VCC Voltage.....8 to 18V

Operation Junction temperature[2)]..... -40ºC to 150ºC

THERMAL PERFORMANCE[3)]

	θ_{JA}	θ_{JC}
QFN4x4-24	131	22ºC/W

Note:

1) Exceeding these ratings may damage the device.

2) JWH3530 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) Measured on JESD51-7, 2-layer PCB ,1OZ.Cu.

ELECTRICAL CHARACTERISTICS

C_{REF}=0.1uF， V_{IN} = 48V,V_{UVLO}=2V,V_{CC}=10V,V_{CS}=0.25V,R_{DLMT}=49.9k Ω， R_{DT}=100 k Ω,R_T=15.4 k Ω,for typical values T_J= 25ºC,for min/max values, T_J is -40 ºC to 125 ºC, unless otherwise stated.

Item	Symbol	Condition	Min.	TYP.	Max.	Units
Startup Section (VIN Pin)						
Startup Circuit Output Current	I_{START}	V_{CC}=V_{CC_ON}-0.2 V ,Vin=48V	40	55	-	mA
Startup Circuit Leakage Current	$I_{Vin(off)}$	V_{IN}=120 V	-	-	100	uA
Minimum Startup Voltage	$V_{in(MIN)}$	V_{CC}=V_{CC_ON}-0.2 V, I_{START}=15mA	-	-	15	V
Supply Voltage Section (VCC Pin)						
Turn-On Threshold Voltage	V_{CC_ON}	VCC Rising	9.1	9.5	9.9	V
Lower Threshold Voltage at 1ST DSS Mode	V_{CC_OFF1}	VCC Falling	9.0	9.4	9.8	V
Higher Threshold Voltage at 2nd DSS Mode	V_{CC_ON2}	VCC Falling	7.4	7.6	7.8	V
Lower Threshold Voltage at 2nd DSS Mode	V_{CC_OFF2}	VCC Falling	7.3	7.5	7.7	V
Turn-Off Threshold Voltage	V_{CC_MIN}	VCC Falling	6.2	6.5	6.8	V
Reset Voltage	VCC_RESET	VCC Falling	6.1	6.4	6.7	V
Startup Delay	tdelay(start)	Delay from VCC(on)to Enable	30	-	125	us
Disabled mode current	ICC_Disable	VUVLO<0.4 V	-	-	2	mA
Standby	ICC_stb	VCC= 10 V, VUVLO= 1 V	-	-	2	mA
No Switching	ICC_No_Sw	VCC= 10 V, ICOMP= 850 µA	-	-	4	mA
Operating Supply Current	ICC_OP	f = 200 kHz, COUTM= COUTA= open	-	-	5	mA
Reference Voltage Section (REF & REFA Pin)						
Reference Voltage	VREF	IREF= 0 mA	4.9	5.0	5.1	V
Load Regulation	VREF(load-reg)	IREF= 0 to 10 mA	4.85	5.00	5.15	V
Step Load Response	VREF(step-reg)	IREF= 5 to 10mA, di/dt= 100 mA/µs	4.85	5.00	5.15	V

Source Current	IREF(MAX)	VREF= 4.75 V	12	-	-	mA
Minimum Decoupling Capacitance	CREF		0.1	-	-	uF
Reference Under Voltage Threshold	VREF(UVLO)	VREF increasing	-	4.5	4.75	V
Reference Under Voltage Hysteresis	VREF(HYS)	VREF decreasing	-	200	-	mV
Line Voltage UVLO Section (UVLO Pin)						
Standby Threshold	VSTBY	VUVLO increasing		0.4		V
Standby Hysteresis	VSTBY(HYS)	VUVLO decreasing		100		mV
Standby Filter Delay	TSTBY(delay)			1.5		us
Enable Threshold	Venable	VUVLO increasing	1.23	1.25	1.27	V
Disable Filter Delay	Tenable(delay)	VUVLO= Venable– 400 mV	0.5	-	1	us
Pull−Down Current in Standby Mode	ISTBY	VUVLO=Venable– 0.1 V VSHDN< VUVLO< Venable	18	20	22	uA
Main Gate Drive Section (OUTM Pin)						
Rise Time (10−90%)	TOUTM(rise)	from 10 to 90% of VOUTM, COUTM= 2.2 nF	-	8.8	17.6	ns
Fall Time (90−10%)	TOUTM(fall)	from 90 to 10% of VOUTM, COUTM= 2.2 nF	-	6	12	ns
Source Current Capability	IOUTM(SRC)	VOUTM= 4 V	2	-	-	A
Sink Current Capability	IOUTM(SNK)	VOUTM= 4 V, VCC= 7.5 V, ICOMP= 850 μA	3	-	-	A
High State Voltage Offset	VOUTM(offset)	VCC –VOUTM VCC= 8 V,COUTM= 2.2 nF	-	-	0.2	V
Low Stage Voltage	VOUTM(low)	VUVLO= 1 V	-	-	0.2	V
Active Clamp Gate Drive Section (OUTA Pin)						
Rise Time (10−90%)	TOUTA(rise)	from 10 to 90% of VOUTA, COUTA= 2.2nF	-	8.8	17.6	ns

Fall Time (90−10%)	TOUTA(fall)	from 90 to 10% of VOUTA, COUTA= 2.2nF	-	17.6	35.2	ns
Source Current Capability	IOUTA(SRC)	VOUTA= 4 V	2	-	-	A
Sink Current Capability	IOUTA(SNK)	VOUTA= 4 V, VCC= 7.5 V, ICOMP= 850μA	1	-	-	A
High State Voltage Offset	VOUTA(offset)	VCC –VOUTA VCC= 8 V,COUTA= 2.2nF	-	-	0.2	V
Low Stage Voltage	VOUTA(low)	VUVLO= 1 V	-	-	0.2	V
Current Sense Section (CS Pin)						
Average Current Limit Threshold	VILIM(ave)		288	300	312	mV
Average Current Limit Leading Edge Blanking Duration	TILIMAVE(LEB)		23	30	37	ns
Average Current Limit Propagation Delay	TILIMAVE(delay)		-	40	-	ns
Cycle by Cycle Current Limit Threshold	VILIM		432	450	468	mV
Over Current Timer when VILIM is reached	TOVLD		150	180	-	ms
Current Sourced by CS low line	ICS_OVPL	VUVLO= 1.4 V	-	0	-	uA
Current Sourced by CS high line	ICS_OVPH	VUVLO= 2.8 V	90	100	110	uA
Cycle by Cycle Current Limit Leading Edge Blanking Duration	TILIM(LEB)		42	55	68	ns
Cycle by Cycle Current Limit Propagation Delay	TILIM(delay)		-	40	56	ns
Short Circuit Current Limit Threshold	VILIM(SC)		679	700	721	mV
Short Circuit Current Limit Leading Edge Blanking Duration	TILIMSC(LEB)		23	30	37	ns
Short−Circuit Current Limit Propagation Delay	TILIMSC(delay)		-	40	56	ns

Short Circuit Counter	NILIMSC		-	2	-	-
Discharge Switch On Resistance	RCS_SW(on)		-	-	35	Ω
Over-Temperature Protection Section (OTP Pin)						
Over temperature Detection Threshold	VOTP(TH)	VOTP increasing	1.23	1.25	1.27	V
Over temperature Detection Delay	TOTP(delay)	VOTP= VOTP(TH) – 20 mV	10	20	30	us
Pull−up Current in OTP Mode	IOTP	VOTP= VOTP(TH) + 0.1 V	18	20	22	uA
Over-Voltage Protection Section (OVP Pin)						
Overvoltage Detection Threshold	VOVP(TH)	VOVP increasing	1.23	1.25	1.27	V
Time Constant to Confirmation	TOVP(TH)		-	0	-	us
Hysteresis current	IHYS	Active when OVP is acknowledged	18	20	22	uA
Soft Start Section (SS Pin)						
Soft−Start Charge Current	ISS	VSS = 1.5 V to 3 V	18	20	22	uA
Soft−Start Onset Threshold	VSS(offset)		-	1.35	-	V
Clamp Voltage	VSS(clamp)		-	0.85	-	V
Discharge Switch On Resistance	RSS_SW(on)	VSS= 100 mV	-	-	30	Ω
Disable Threshold	VSS(disable)	VSS decreasing	0.4	0.5	0.6	V
Restart Section (RES Pin)						
Restart Delay Threshold	VRES(TH)	VRES increasing	0.96	1.00	1.04	V
Peak Voltage	VRES(peak)	VCS > VILIMAVE, VRES increasing	3.8	4.0	4.2	V
Valley Voltage	VRES(valley)	VCS > VILIMAVE, VRES decreasing	1.9	2.0	2.1	V
Discharge Current	IRES(SNK)	VCS < VILIMAVE, VRES =100mV	4	5	6	uA
Charge Current	IRES(SRC1)	VCS > VILIMAVE,VRES= VRES(TH) – 50 mV	18	20	22	uA
	IRES(SRC2)	VCS > VILIMAVE,VRES= VRES(TH) + 50 mV	4	5	6	uA

Restart Counter	nRES	VOTP> VOTP(TH)		32		-
Discharge Voltage	VRES(DIS)		50	100	150	mV
Discharge Switch On Resistance	RRES_SW(on)	VRES= 200 mV	-	-	110	Ω
Fault report and Remote Shutdown Section (FLT/SD Pin)						
Enable Threshold	VFLT(enable)	VFLT/SD= increasing	1.37	1.45	1.53	V
Fault Threshold	Vfault_FLT/SD	VFLT/SD= decreasing	1.23	1.25	1.27	V
Internal Pull−Up Resistor	RFLT/SD	VFLT/SD= 3 V	8.5	10.0	11.5	kΩ
Discharge Switch On Resistance	Rfault_SW(on)	VFLT/SD= 100 V	-	-	120	Ω
Oscillator Section (RT Pin)						
Operating Frequency Range	frange		100	-	1000	kHz
Oscillator Frequency (tD ≈100 ns)	fOSC1	RT= 16.3 kΩ, RDT=46.86kΩ, RDLMT= 75.5 kΩ	186	200	214	kHz
Oscillator Frequency (tD ≈50 ns)	fOSC2	RT= 7.96 kΩ, RDT=23.43kΩ, RDLMT= 37.6kΩ	372	400	428	kHz
Synchronization Section (Sync Pin)						
Sync Pin Input Voltage to “1” level	VsyncH	Acknowledged high level	2.8	3	3.4	V
Sync Pin Input Voltage to “0” level	VsyncL	Acknowledged low level	1.4	1.6	1.8	V
Sync Input Pulse Width	tsync_iw	Minimum input width for proper sync operation	50	-	-	ns
Sync Pullup Current	IsyncPU		0.45	0.6	0.75	mA
Sync Pulldown Current	IsyncPD		1.4	1.6	1.8	mA
Sync Permanent Pulldown Current	IsyncPPD		26	32	38	uA
Sync Output Width	tsync_ow	Output Pulse Width	130	180	230	ns

Sync to Output Delay	tsync_delay	Rising edge of sync pulse to OUTM rising edge	-	32	50	ns
Maximum Duty Ratio Section (DLIMT Pin)						
Maximum Duty Ratio	D(MAX1a)	f = 200 kHz, RT= 16.3 kΩ, RDT=46.86 kΩ, RDLMT= 75.5 kΩ	76.0	80.0	84.0	%
	D(MAX2a)	f = 400 kHz, RT= 7.96 kΩ, RDT= 23.43 kΩ, RDLMT= 37.6 kΩ	76.0	80.0	84.0	
Minimum Duty Ratio	D(MIN)	ICOMP= 850 μA	-	-	0	%
Ramp Section (RAMP Pin)						
PWM Propagation Delay	TPWM		-	40	60	ns
PWM Offset Voltage	VPWM(offset)		-	1.35	-	V
Discharge Switch On Resistance	RRAMP_SW(on)	VRAMP= 100 mV	-	-	25	Ω
RAMP Input Leakage Current	IRAMP(leak)	VRAMP= 1.8 V	-	-	100	nA
Error Amplifier Section (COMP Pin)						
Mirrored Current Ratio	kcomp			10:1		
COMP Pin Dynamic Resistance	RCOMP1			400		Ω
Mirrored Current Pulls Up Resistance	RCOMP2			50		kΩ
Volt-Second Clamp Section (Vsclamp Pin)						
Volt Second Limit Voltage Threshold	VSLIMIT	ICOMP= 0 μA	1.44	1.50	1.56	V
Volt−Second Propagation Delay	tVSCLAMP	Step VSCLAMP to 2 V to OUTM falling edge, dV/dt = 10 V/μs	-	40	60	ns
VSCLAMP Switch On Resistance	RVSCLAMP_SW(on)	VSCLAMP= 100 mV	-	-	45	Ω
VSCLAMP Input Leakage Current	IVSCLAMP(leak)	VSCLAMP= 1.4 V			100	nA
OverlapTime Delay Section (DT Pin)						

Overlap Delay Range	tD(range)		20		500	ns
Overlap Delay from OUTA to OUTM rising Edges	tDa	RDT= 46.86kΩ, VCS= 0.4 V	75	100	125	ns
	tDb	RDT= 46.86 kΩ, VCS= 50 mV	93	124	155	
	tDc	RDT= 23.43kΩ, VCS= 0.4 V	37.5	50	62.5	
	tDd	RDT= 23.43 kΩ, VCS= 50 mV	46	62	78	
Thermal Shutdown						
Thermal Shutdown		Temperature increasing		165	-	℃
Thermal Shutdown Hysteresis	TSHDN(HYS)	Temperature decreasing	-	20	-	℃

PIN DESCRIPTION

Pin	Name	Description
1	RAMP	PWM modulator ramp. In voltage mode an external R−C circuit from Vin sets the PWM Ramp slope to implement feed-forward. In current mode control, the resistor of the external R−C circuit connects to REF for ramp compensation.
2	SS	Soft−start control. Duty ratio is limited during startup by comparing the voltage on this pin to a level−shifted VSCLAMP signal. Under steady state conditions, the SS voltage is approximately 4.5 V. Once a fault is detected the SS capacitor is discharged and the controller is disabled.
3	DLIMT	Maximum duty ratio limit.
4	DT	Dead time control.
5	RT	Oscillator frequency setting pin.
6	AGND	Analog circuit ground reference.
7	COMP	Input to the pulse width modulator. An external optocoupler connected between the REF and COMP pin sources current into an internal current mirror.
8	RES	Restart time control. A capacitor between this pin and AGND set the shutdown delay and hiccup mode restart delay time.
9	OVP	Over-voltage protection. When this pin is biased beyond 1.25 V, all pulses immediately stop and the controller resumes operations after 32 VRES charge/discharge cycles.
10	CS	Current sense input. The current sense signal is used for current−mode control, adaptive dead time control, cycle−by−cycle current limiting, over−current protection and short circuit protection, etc.
11	REF	Precision 5 V reference. Maximum output current is 12 mA.
12	OTP	Over−temperature protection. A voltage divider containing a NTC connects to this pin.
13	VCC	Positive input supply.
14	OUTM	Main switch gate control. OUTM can source 2 A and sink 3 A
15	PGND	Ground connection for OUTM and OUTA.
16	OUTA	Active clamp switch gate control. OUTA can source 2 A and sink 1 A.
17	$\overline{\text{FLT}}/\text{SD}$	Fault report and shutdown control. This is a dual−function bi−directional pin.

18	REFA	Internally connected to REF.
19	UVLO	Input voltage under voltage detector. By monitoring the voltage on the UVLO pin, the controller can be put in three different modes: disable, standby and enable.
20	SYNC	This bi−directional pin is used to synchronize the controller or synchronize another controller driven by this pin.
21	NC	No connect (creepage distance)
22	VIN	High voltage startup circuit input.
23	NC	No connect (creepage distance)
24	VSCLAMP	Volt−second clamp. An external R−C divider from the input line generates a voltage ramp.

FUNCTIONAL DESCRIPTION

The JWH3530 is a highly−integrated dual−mode active clamp PWM controller targeting next−generation high−density, high−performance and small to medium power level isolated dc−dc converters for use in telecom and datacom applications. Operating up to 1 MHz, the part can be configured in either voltage mode control with input voltage feedforward or peak−current mode control. An adjustable adaptive overlap time between the main power and the active clamp MOSFETs optimizes system efficiency based on load conditions enabling higher efficiency and greater power density solutions.

This controller integrates all the necessary control and protection functions to implement an isolated active−clamp forward or asymmetric half−bridge converter with synchronous rectification. It integrates a high−voltage startup bias regulator directly connected to the dc input up to 120 V.

1. Start-Up

1.1. HV Start-Up

The JWH3530 integrates a high voltage startup circuit accessible by the VIN pin. The startup circuit is rated up to a maximum voltage of 120 V. The startup regulator consists of a constant current source that supplies current from a high−voltage rail to the capacitor on the VCC pin (CVCC). The startup circuit current is 40 mA minimum. The internal high voltage startup circuit eliminates the need for external startup components. In addition, this regulator reduces no−load power and increases the system efficiency as it uses negligible power in the normal operation mode.

The startup circuit is configured to operate in the Dynamic Self−Supply (DSS) mode in certain conditions. There are two DSS modes. In the first DSS mode, Vcc hiccups between two levels (9.5 and 9.4 V typically) and self-supplies the IC. This mode can be briefly entered at startup (fault clearance delay).The DSS block maintains the controller supply until the part is ready to switch when all faults are cleared.

At the end of the initialization sequence, the controller stops the high−voltage startup source and Vcc drops as the auxiliary voltage did not build up yet. If the auxiliary winding does not take over the controller supply when VCC reaching the lower regulation threshold, VCC(off2), typically 7.5 V, the 2nd DSS takes place. In the second DSS mode, Vcc hiccups between two levels (7.5 and 7.6 V) and self-supplies the IC. The HV startup operation waveform is as figure 4.

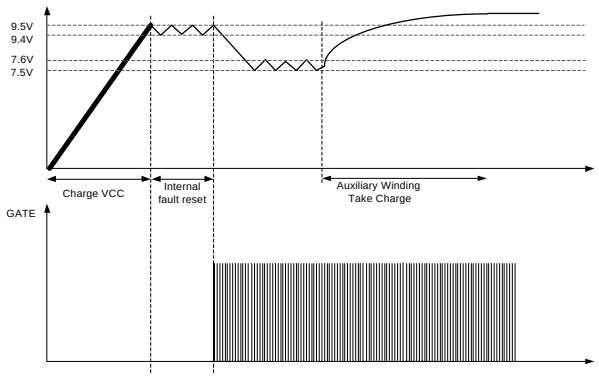


Figure 4. HV start up operation

2. Normal Operation

2.1 PWM control

To get a faster system response, a current−based feedback input is adopted.

The PWM comparator modulates the duty ratio to regulate the output voltage. A signal proportional to the loop error signal is applied to this pin using an opto-coupler. A voltage proportional to the error signal, VERROR, is internally generated and compared to a regulation ramp. The on−time terminates once the ramp exceeds the internal error voltage.

The internal error voltage is generated by applying a current into the COMP pin as shown in Figure 5. The COMP current is internally mirrored

with a 10:1 ratio. The mirrored current pulls down on a 50k pull−up resistor from 5V supply.

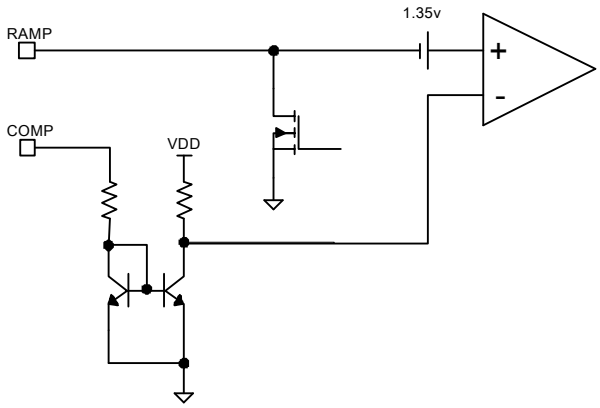


Figure 5. PWM control

2.2 Volt−Second Clamp

A volt−second clamp is an important safety feature in any forward converter, especially active clamp type where the duty ratio can easily exceed 50%. A clamp helps preventing magnetizing current runaway and transformer saturation in faulty situations. An external RC divider (RVSCLAMP−CVSCLAMP) from the input line generates the VSCLAMP ramp to control the volt−second limit of the converter. The slope of the ramp is proportional to the input voltage and controls the maximum on−time during a line voltage transition. The ramp prevents from exceeding the maximum volt−second of the transformer by clamping the duty ratio during the transient input. Figure 6 shows the recommended clamp configuration.

The PWM drive pulse terminates once the VSCLAMP ramp reaches VSLIMIT, typically 1.5 V. The RC divider is selected such that the VSCLAMP ramp peak voltage reaches VSLIMIT at the desired maximum volt−second limit. The VSCLAMP pin is pulled down by SWVSCLAMP at the end of every cycle and is held low until the next drive pulse.

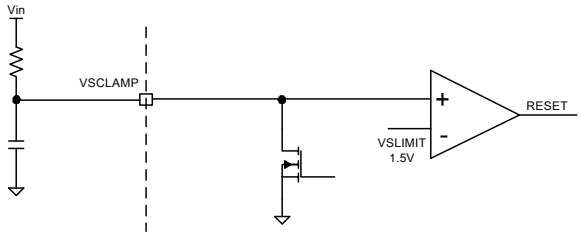


Figure 6. Volt−Second Clamp

2.3 Frequency and Maximum Duty Ratio

The oscillator frequency (FSW) and The maximum duty ratio of the oscillator(Dmax) are set by RT and RDLMT which are placing between AGND pins and RT&RDLMT respectively.
JWH3530 is optimized for operation between 200 kHz and 1 MHz. The adjustable duty ratio range is between 50 and 80%. The maximum duty ratio accuracy is ±3%.

Equation 1 and 2 show the relationship between FSW & Dmax and RT&RDLMT.

$$\frac{D_{max}}{F_{sw}} = R_{DLMT} \times 54p - T_d + 20n \quad \text{(eq. 1)}$$

$$\frac{(1-D_{max})}{F_{sw}} = R_T \times 54p + T_d + 20n \quad \text{(eq. 2)}$$

Where Td at above equations is the overlap time between main NMOS and active clamp PMOS.

2.4 Soft Start

Soft−start slowly increases the duty ratio during power up, allowing the controller to gradually reach steady−state operation by slowly increasing the output voltage while reducing startup circuit stress. The duty ratio is controlled by comparing the SS pin voltage to the voltage which is 1.35V level−shifted by VSCLAMP as figure 7.

VSS is slowly increased by charging the soft−start capacitor with a fixed current source, ISS, typically 20 μA. The soft−start pin is internally grounded while a fault is present.

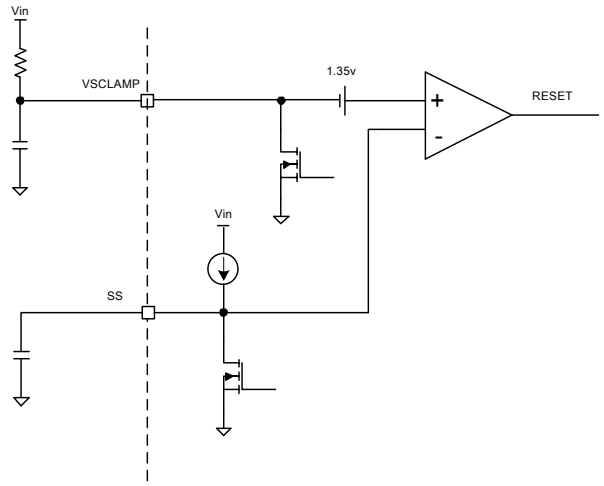


Figure 7. Soft start

2.5 Active−Clamp MOSFET Turn−off Sequence

JWH3530 drives an external P−type MOSFET through a capacitive link via the OUTA pin. During the power off sequence, the OUTA pin will remain high and follow the VCC as it slowly discharges. This is to avoid observing a glitch in the output voltage if OUTA would go low at the VCC under−voltage lockout point.

2.6 Drive overlap time

In an active clamp forward converter, there are two delays involved in the driving signals. Both deal with Zero Voltage Switching (ZVS) operations.

A simplified block diagram and waveforms of an active clamp forward converter with a low side active clamp switch are shown in Figure 8. Driver OUTM drives the main switch while OUTA drives the active clamp switch. Overlap time between the drive signals is required to achieve zero or near zero volts switching (ZVS) on the switches.
The drive overlap time is usually optimized for efficiency. However, the optimum overlap time required to achieve ZVS varies with line and load conditions. JWH3530 adaptively adjusts the overlap times to optimize the system efficiency across operating conditions. The current sense information (representative of load) is used to adjust the overlap times. The overlap times are essentially constant at medium to high load. In light load conditions, overlap times are inversely proportional to load current. The adaptive overlap time adjustment becomes active around 30 % of the maximum load.

A resistor, RDT, between the DT and AGND pins adjusts the overlap time. The minimum delay is 20 ns. Equation 3 shows the relationship between overlap delays and RDT, current sense voltage.Td1 equals to Td2.

$$t_D(V_{CS}) = \frac{R_{DT}\times 1.66\times 10^{-16}}{Min\left(\frac{V_{CS}}{2k}, \frac{1.4V}{35k}\right)+\frac{1.4V}{37k}} \quad \textbf{(eq. 3)}$$

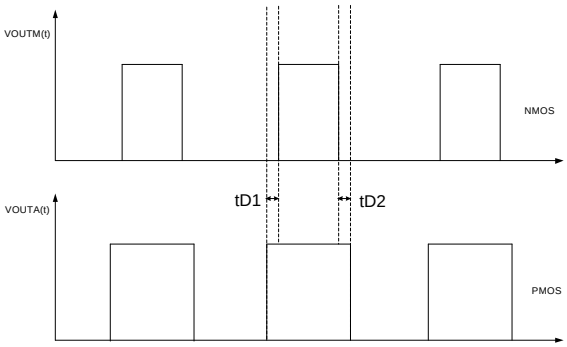


Figure 8. PMOS and NMOS drive overlap

3. Protection

3.1 Input under voltage protection

JWH3530 monitors the line voltage and enables the controller when the input voltage is within the required range. The input voltage is sampled using a resistor divider. The UVLO input can also be used as an enable/disable function.

By monitoring the voltage on the UVLO pin, the controller can be put in three different modes: standby, disable and enable. The controller enters standby mode once the UVLO voltage, VUVLO, exceeds the standby threshold, VSTBY, typically 0.4 V. The standby mode features a 100 mV hysteresis. In standby mode, VCC hiccups between 9.5 and 9.4 V, the reference voltage is maintained, and the FLT/SD pin is pulled low.
The controller enables once VUVLO exceeds

Venable, typically 1.25 V. Once in enable mode, the controller is allowed to start if no other faults are present. An internal pull−down current source, which is typically 20 μA, provides hysteresis.

The block diagram of input under voltage protection is shown as

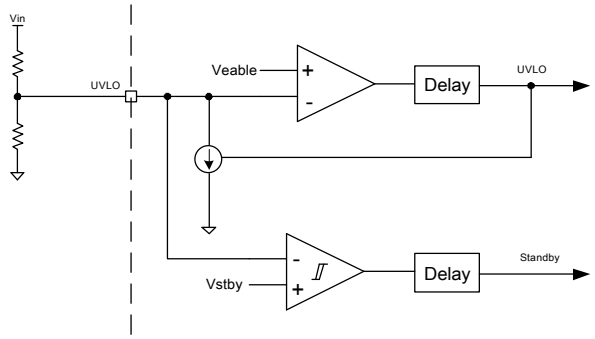


Figure 9. Input under voltage protection

3.2 Current sense related protection

A signal proportional to the current across the main switch is applied to the CS pin. The current sense information is used to calculate the average primary current to modulate the drivers overlap time and implement overcurrent protection (OCP). It is also used for cycle by cycle peak current limit control and detecting a short circuit condition. Figure 10 shows the block diagram of the current sense related protection.

- Regular current pulse: in a forward converter normal operation, the primary current is made of the reflected inductor current to which adds the primary magnetizing current. When the voltage image of this current exceeds the feedback set point (in current mode) or the maximum sense voltage (0.45 V typical in voltage mode), the current pulse is terminated. When this comparator trips, a 150ms fault timer starts counting and shuts the controller down upon completion if the overload remains present
- Short−circuit pulse: if an abnormally−high current pulse is detected (0.7 V) for two consecutive pulses, the part shuts off and goes into restart mode. This can happen during a winding short circuit or in presence of a defective component in the secondary side
- Overcurrent condition: in case the converter's output is overloaded, the average input current will increase, reflecting output power increase. The JWH3530 averages the primary−side current sense information and when it exceeds a certain value, a shutdown delay starts. When this delay elapses, the part shuts off and goes into restart mode

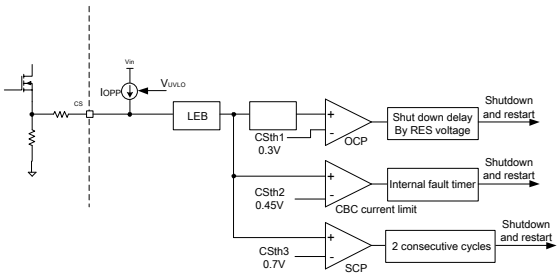


Figure 10. Current sense related protection

3.3 Over Power Compensation

The accuracy of OCP is related to the gate turn-off delay and the accuracy of sampled average current. To compensate the OCP difference at different line, a current source is connected to the CS pin and sources current out of the pin. This is what is shown in Figure 11.

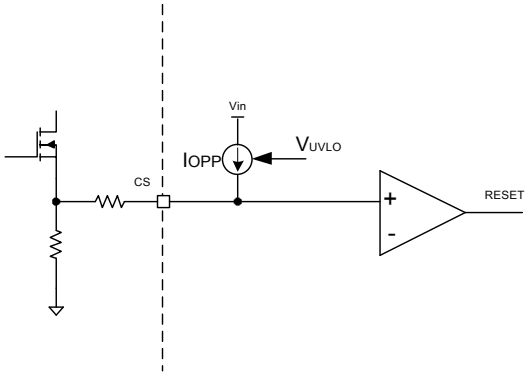


Figure 11. Over power compensation

In Figure 12, you can see the curve linking the current source value and the UVLO level. Below 1.4V UVLO voltage, the offset current is 0A and there is no over power compensation. As the

UVLO voltage increases, the offset current also grows and builds an offset on the CS pin. This current offset is 100uA maximal limitation when UVLO voltage is higher than 2.8V.

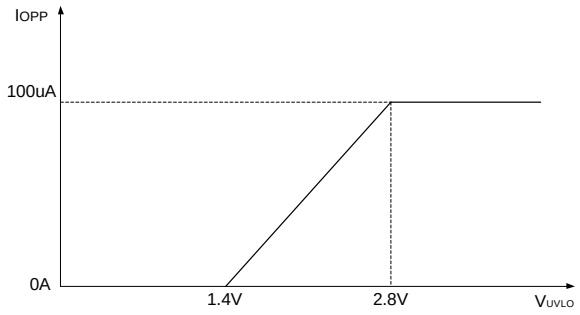


Figure 12 Over power compensation current curve

3.4 Over Voltage Protection

The circuit includes an auto−recovery over voltage protection pin. When this pin is above 1.25 V typically, it immediately stops switching pulses and forces an auto−restart mode. At that moment, a 20 μA current source activates and lifts the pin to provide hysteresis. At the end of the auto−restart mode, the controller monitors the OVP pin and if its voltage has gone back below 1.25 V, the IC resumes operations.

3.5 Over Temperature Protection

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled without a shutdown pulse if the junction temperature exceeds the thermal shutdown threshold, TSHDN, typically 165C. The controller restarts once the IC temperature drops below TSHDN by the thermal shutdown hysteresis, TSHDN(HYS), typically 20C and VCC has charged to VCC(on) at least once while in thermal shutdown mode. A thermal shutdown fault is cleared if VCC drops below VCC(reset), or if VUVLO falls below VSTBY by its hysteresis level. A power−up sequence commences at the next VCC(on) if all faults are removed.

3.6 Restart Mode

The JWH3530 incorporates a restart timer to disable the controller for a certain amount of time and initiate a hiccup mode operation if a fault is detected. In short circuit operations, this technique limits the overall dissipated power. Once the fault is gone, the controller automatically resumes operations. A restart event occurs if one of the following faults is detected:

Overcurrent fault (OCP)

Overvoltage fault (OVP)

Two consecutive short−circuit pulses (SCP)

Over temperature fault detected on OTP pin

Internal thermal shutdown fault

The FLT/SD pin has been externally pulled low

The simplified architecture of the restart timer is shown in Figure 13.

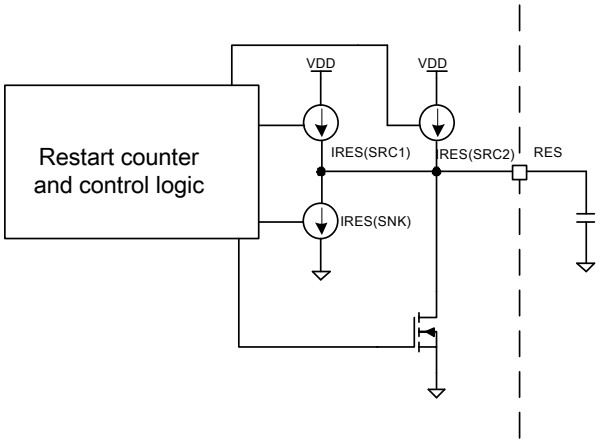


Figure 13. Restart timer

A pull−down current source, IRES(SNK), typically 5 μA, holds the RES pin at a low level when no faults are present. When fault happens, the restart timer sequentially charges and discharges the capacitor on the RES pin 32 times, between 2 V and 4 V to set the restart or hiccup duration.

The RES pin combines two functions: the restart delay and the shutdown delay.

The shutdown delay is actually the time taken by the RES pin to charge from 0 to 1 V. The shutdown delay is only activated at overcurrent fault. This charge is initiated by the average input current reconstruction. When this internal averaged current exceeds 0.3 V, the capacitor on

the RES pin is charged by the 20 µA source, which is named IRES(SRC1) . If the over current goes away, the capacitor slowly discharges via a 5 µA pull−down current sink, which is named IRES(SNK). If the fault comes back, the 5µA sink turns off and the 20 µA is reactivated. When the capacitor voltage eventually reaches 1 V, all pulses are stopped, and the part enters auto−recovery hiccup mode via the restart delay.

The restart delay is made of 32 up/down cycles between 2V and 4 V on the RES pin. The charge and discharge current is 5µA pull−up current source and 5 µA pull−low current source which correspond to IRES(SRC2) and IRES(SNK) respectively. The restart mode ends after 32 consecutive charge/discharge cycles. C_{RES} is then pulled low using an internal pull down transistor, SW_{RES}. The transistor is disabled once VRES falls below the discharge level, $V_{RES(DIS)}$, typically 100 mV. Once C_{RES} is fully discharged a new startup sequence commences and soft−start is released.

During the restart delay, the VCC pin is maintained by the controller operating the high−voltage current source in the DSS mode: the voltage hiccups between 9.4 and 9.5 V.

3.7 Fault Reporting and Shutdown Input

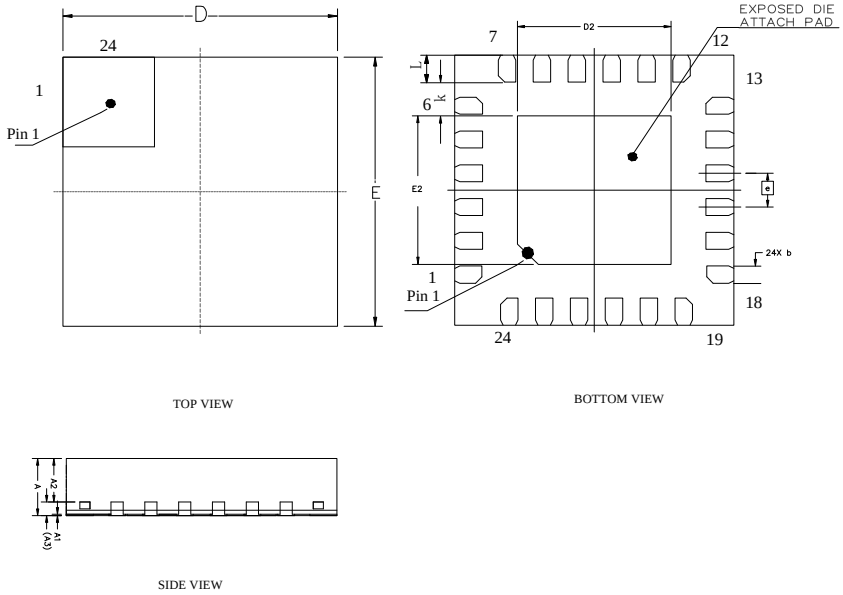
The FLT/SD pin reports the presence of a fault to an external supervisory circuitry. It also can be used to shut down the controller if externally brought down. This pin has an open collector output with a 10 kΩ internal pull−up resistor (RFLT/SD) connected to the 5V reference. The FLT/SD pin is internally pulled low (to indicate a fault) by an internal transistor, , when an overcurrent, short circuit, VCC(UVLO), OVP, OTP or low input voltage fault is detected. The pin is also pulled low when the controller is in restart mode.

During the initialization sequence, the shutdown detection pin is released once Vref reaches its regulation level. The controller considered that the FLT/SD pin is cleared from a fault when the pin voltage, VFLT/SD, exceeds the enable threshold, VFLT(enable), typically 1.45 V, and VSS exceeds VSS(disable), typically 0.5 V. The controller is disabled once VFLT/SD, falls below the shutdown threshold, Vfault, typically 1.25 V. While the controller is in shutdown state, VCC is hiccupping between 9.5/9.4 V typically and VREF is kept high. When the FLT/SD pin is brought low, the part activates the restart delay (RES is cycled up and down 32 times) before a new restart is authorized when the FLT/SD pin is released.

Figure 14 gathers all the possible events that can activate the fault pin. **Shutdown Cause**	**Auto−Recovery**	**Shutdown Delay**	**Restart Delay**	**Pull Low FLTSD Internally**
V_{IN} < V_{ENABLE}	Yes	No	No	Yes
V_{IN} < $V_{STANDBY}$	Yes	No	No	No
V_{CC} < $V_{CC(MIN)}$	Yes	No	No	Yes
V_{CC} < $V_{CC(reset)}$	Yes	No	No	No
REF UVLO	Yes	No	No	Yes
OCP	Yes	Yes	Yes	Yes
SCP	Yes	No	Yes	Yes
OTP	Yes	No	Yes	Yes
OVP	Yes	No	Yes	Yes
Built−in Thermal Shutdown	Yes	No	No	Yes
FLT/SD	Yes	No	Yes	Yes
SS low	Yes	No	No	YES

PACKAGE OUTLINE

QFN4X4-24 **UNIT: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	—
A3	0.203REF		
D	4.00BSC		
E	4.00BSC		
D2	2.10	2.20	2.30
E2	2.10	2.20	2.30
k	0.50REF		
b	0.21	0.25	0.31
e	0.50BCS		
L	0.30	0.40	0.50

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