JW7726BH

Synchronous Rectifier Controller

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JW®7726BH is a synchronous rectifier controller, used for the secondary side rectification of isolation topologies, such as Active Clamp Flyback and CCM/QR/DCM Flyback. By driving an external MOSFET, JW7726BH is able to significantly improve the efficiency comparing with the conventional diode rectifier.

When JW7726BH senses V_{ds} of MOSFET less than -140mV, it turns on the MOSFET. Once the V_{ds} is greater than -6mV, JW7726BH turns off the MOSFET.

JW7726BH supports multiple operation modes, such as DCM, CrCM, CCM and Quasi-Resonant. By implementing the Joulwatt proprietary technology, JW7726BH is able to handle CCM operation.

JW7726BH is available in SOT23-6 package.

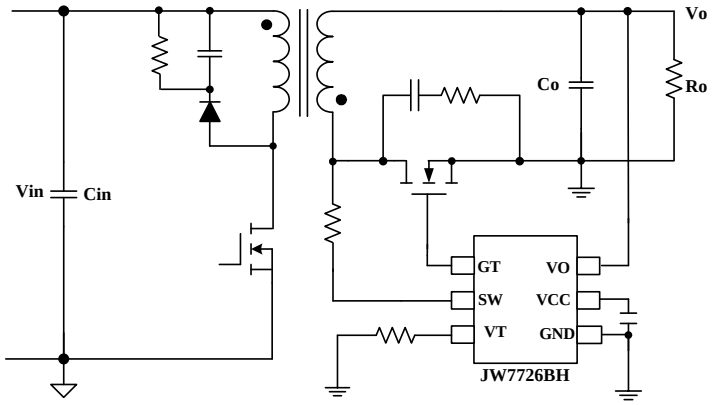
FEATURES

- Supports Active Clamp Flyback, DCM, Quasi-Resonant, and CCM Flyback
- Support High-side and Low-side Rectification
- Output Voltage Directly Supply VCC
- Low Quiescent Current
- Fast Driver Capability for CCM Operation
- SOT23-6 Package

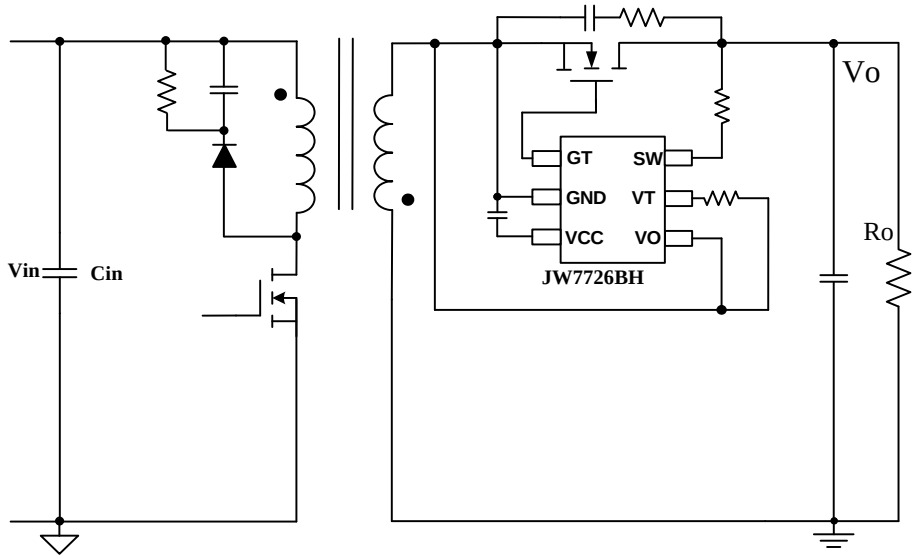
APPLICATIONS

- Active Clamp Flyback and Flyback Converters
- Adaptor
- LCD and PDP TV

TYPICAL APPLICATION



JW7726BH Typical Application for Low-side.

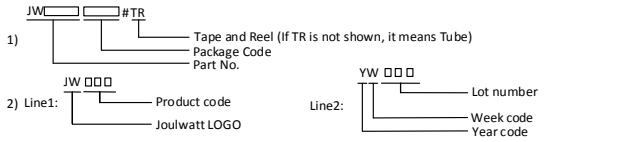


JW7726BH Typical Application for High-side.

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW7726BHSOTB#TR	SOT23-6	JWJ9□ YW□□□	Green

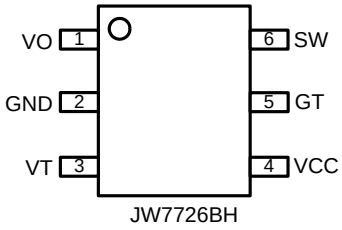
Notes:



3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



JW7726BH

ABSOLUTE MAXIMUM RATING[1)]

SW PIN .....-1 to 150V
VO PIN .....-0.3 to 28V
VCC, GT PIN.....-0.3 to 9V
VT PIN..... ....-0.3 to 7V
Continuous Power Dissipation(T_A=+25℃)[2)] SOT23-6…..….....0.625W
Junction Temperature [3)].....150ºC
Lead Temperature ….....260ºC
Storage Temperature….....-65ºC to150ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS

SW Pin.....4.7V to 130V
VO Pin.....4.7V to 25V
VCC, GT PIN.....4V to 8.5V
Operation Junction Temp. ..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
SOT23-6.....	200	...130ºC/W

Note：

1) Exceeding these ratings may damage the device. These stress rating do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$.

5) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

TA = 25ºC, unless otherwise stated

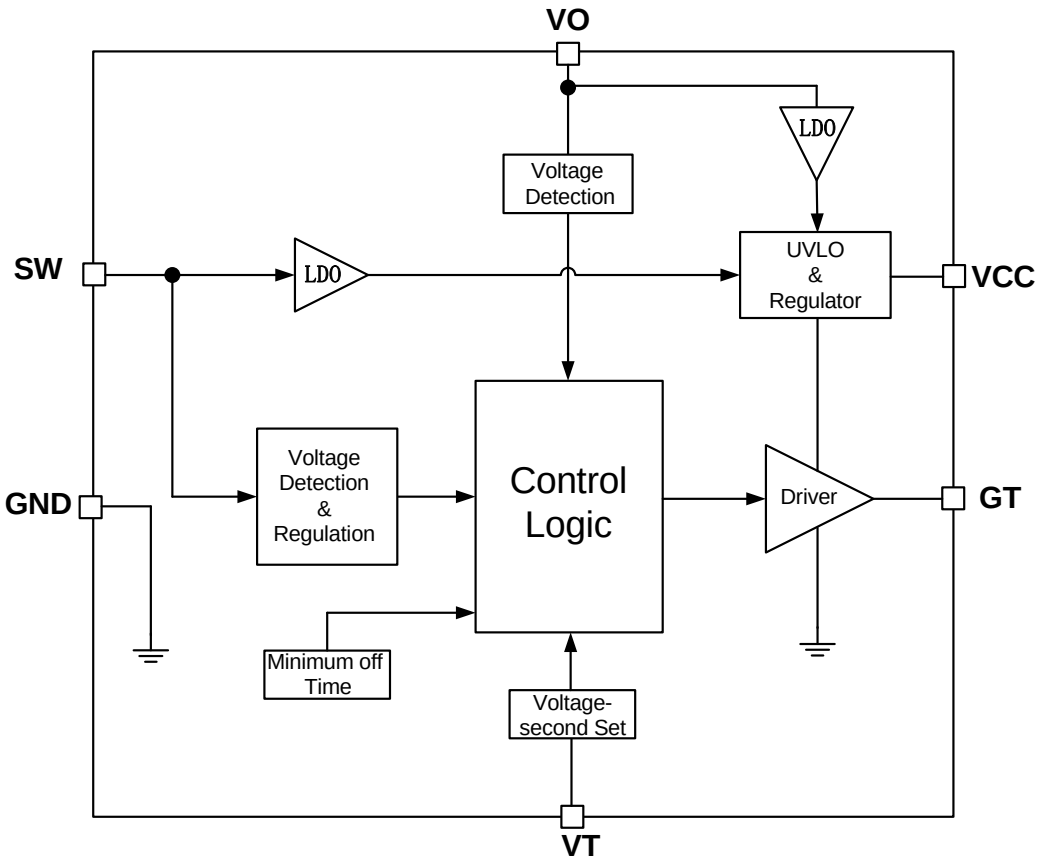
Item	Symbol	Condition	Min.	Typ.	Max.	Units
VCC Section						
VCC Voltage	VCC	SW=40V, VCC=2.2uF	7.4	7.9	8.4	V
VCC Startup voltage	$V_{CC\_Startup}$		4.2	4.5	4.8	V
VCC UVLO	V_{CC_UVLO}		3.7	3.95	4.2	V
Operation Current (GT On)	I_{VCC}	GT=5nF,VCC=2.2uF	0.7	0.9	1.1	mA
Quiescent Current	I_q	VCC=4.5V, VCC=2.2uF	100	120	140	uA
Gate Section						
Gate Turn on Threshold	V_{MOS_ON}		-170	-140	-110	mV
Gate Turn off Threshold	V_{MOS_OFF}		-12	-6	0	mV
Gate Turn on Voltage	V_{GT}	SW=32V, VCC=2.2uF 6)	V_{CC}-0.1	V_{CC}		V
Maximum Gate Pull up current	I_{GU}	VCC=8V, GT=0V to 3V 6)	0.48	0.6		A
Maximum Gate Pull down current	I_{GD}	VCC=8V, GT=5V to 2V 6)	3.2	4		A
Gate Minimum on Time	T_{MIN_ON}		490	540	590	ns
Turn-on total delay	T_{DON}	VCC=8V, C_{LOAD}=4.7nF 6)	44	50	60	nS
Turn-off total delay	T_{DOF}	VCC=8V, C_{LOAD}=4.7nF 6)	16	20	26	nS
SW and VO Section						
Volt-second Threshold 6)	TH_V*us	VT=100KΩ, Volt-second increasing	20.9	24	27.1	V*uS
Volt-second Threshold Hysteresis 6)	TH_hys	VT=100KΩ, Volt-second increasing	24%	25%	26%	
VCC Charge Current	I_{SW_CHG}	SW=40V, VCC=6V	75	95		mA
SW Regulation Voltage	V_{MOS_REG}		-50	-38	-26	mV
SW Control Voltage MAX	$V_{MOS\_REG\_MAX}$		-190	-165	-140	mV
VO Enable Charge Voltage	V_{O_EN}	VCC=4V, SW=0V, rising	4.5	4.65	4.8	V
VO Disable Charge Voltage	V_{O_DIS}	VCC=4V, SW=0V, falling	4.4	4.55	4.7	V
VO Charge Current	I_{VO_CHG}	SW=0V, VCC=6V, VO=12V	28	40	52	mA

6) Guaranteed by design.Not tested in production.

PIN DESCRIPTION

Part No.	Name	Description
5	GT	Drive the External NMOSFET.
2	GND	Ground.
4	VCC	Power supply. Bypass a Capacitor Between VCC and GND.
3	VT	Set the voltage-second product.
1	VO	Output Voltage Sensing and Charging to VCC.
6	SW	External Power MOSFET Drain Voltage Sensing. Charging to VCC.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW7726BH is a synchronous rectifier controller which combined with external MOSFET can replace the Schottky Barrier Diode. It supports all operations, such as DCM, CrCM, (Quasi-Resonant) and CCM when adopted in Active Clamp Flyback and Flyback converters.

Startup

During the startup period, when the VCC is charged up by the two internal LDOs connected to SW and VO pin respectively.

When VO is lower than 4.55V (falling), JW7726BH can power itself through the internal LDO connected to SW pin during the SR turn-off period, which means primary the primary side MOSFET is turned on and SW presents a positive voltage. A capacitor between VCC and GND is required to store the energy and supply to IC during the SR turn-on period.

When VO is above 4.65V (rising), the VO pin charges VCC pin.

Once the VCC voltage exceeds $V_{CC\_Startup}$, the JW7726BH exits the UVLO. If VCC is lower than V_{CC_UVLO}, the external MOSFET is turned off. The current flows though body diode before the VCC reaches to the startup voltage $V_{cc\_startup}$.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and pulled low internally. Once the VCC exceeds the startup voltage Vcc_startup, the parts is activated again.

Turn On Phase

There are two conditions for the JW7726BH to turn on the SR, i.e. Vsw, voltage-second value on SW pin when primary side switch is on, and the turn on phase is shown in Fig. 1.

1) Vsw: when the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage V_{SW} across it. When V_{SW} is lower than V_{MOS_ON}, the part will pull the gate high to turn on the synchronous MOSFET after turn on delay time T_{DON} if the other condition is met.

2) Volt-second of SW: in DCM and QR operation, there are parasitic oscillations. In some applications, the drain resonant voltage may fall below the SR turn on threshold, especially for the first couple rings. SR could be falsely turned on, which may cause shoot through issue and result in high power loss. The volt-second value of SW pin can be used to distinguish the parasitic ring from normal primary side switch on. The threshold can be set by the resistance at VT pin. The curve is shown in Fig. 2.

In application, as the output load(Io) of converter increases, the volt-second value(S1) of SW pin also increases. When the volt-second value(S1) of SW pin is greater than the high threshold and gate turns on, the high threshold becomes to low threshold. As the output load decreasing, when the gate turns off and the MOSFET bodydiode conduction time is no shorter than Ton_min., the low threshold becomes to the high threshold. When the Rvt is more than 250kΩ, the high threshold is fixed and the low threshold increases with the increasing of Rvt. The low threshold is fixed and equal to the high threshold when the Rvt is more than 330kΩ. The voltage-second hysteresis is shown in Fig. 2 and Fig. 3.

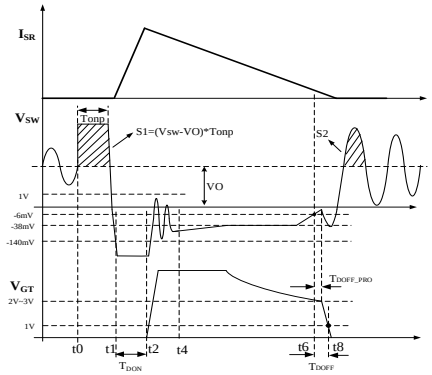


Fig. 1 Turn on delay and turn off delay

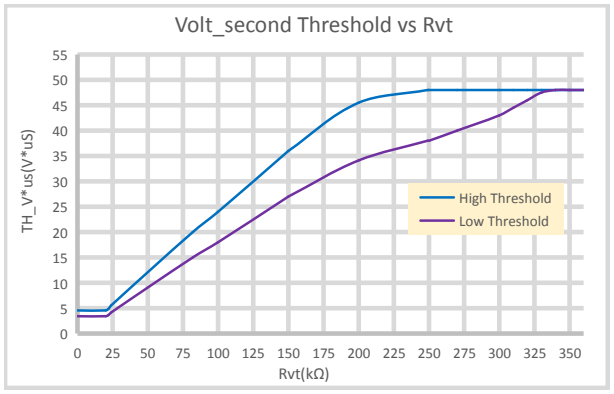


Fig. 2 Volt-second value vs. VT resistance

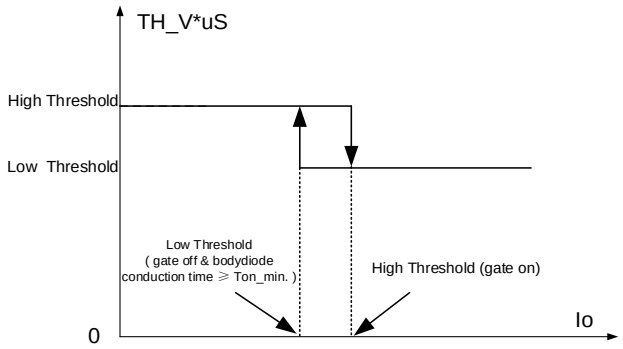


Fig. 3 Volt-second value with hysteresis

Minimum On Time (MOT)

When the synchronous MOSFET is turn on, there is a minimum on time for the SR. The V_{SW} voltage may have a parasitic ring when the synchronous MOSFET turns on. So, a minimum on time (MOT) is very important to avoid the MOSFET turn off threshold is false triggered. Minimum on time is 510ns for high frequency applications.

Conducting Phase

When the synchronous MOSFET is turned on, the drain source voltage Vsw it is determined by its on resistance and the current through it. The part adjusts the gate voltage and regulates the Vsw to the internal threshold (typical -38mV) after the synchronous MOSFET turn on. When the V_{SW} is lower than -38mV, the gate keeps its maximum voltage. And the synchronous MOSFET is fully on.

The Vsw rises when the current follow through the MOSFET decreases. The gate voltage will be decreased to increase its on resistance and regulate the Vsw around -38mV.

It should be noted that the typical regulation threshold (-38mV) during MOSFET on time is not fixed, it can be internally changed to ensure the proper operation under CCM mode.

Turn Off Phase

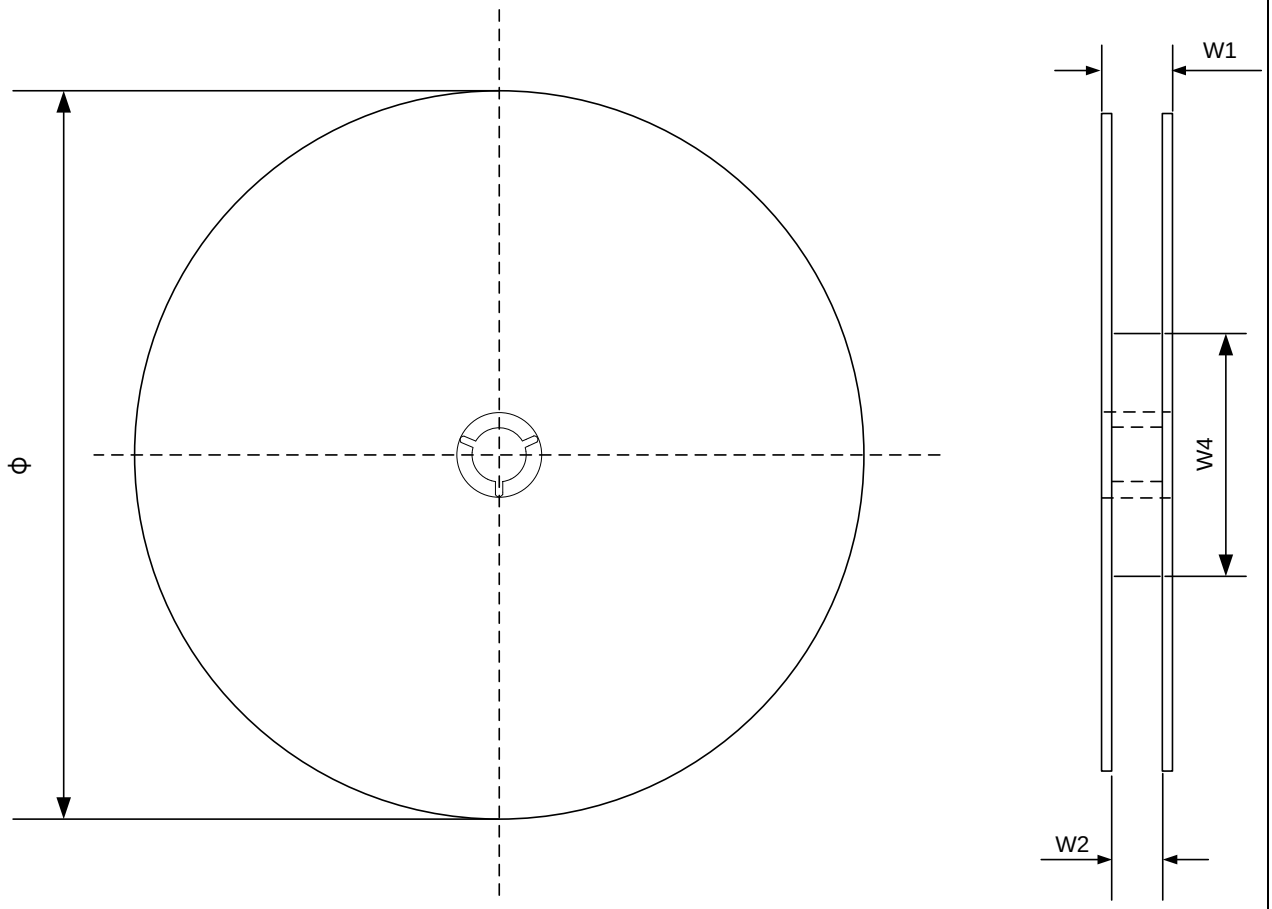
After synchronous MOSFET conducting, once the voltage VSW touches the MOSFET turn off threshold (-6mV), the gate is pulled to low after a turn off delay time TDOFF. A 330nS blanking time is necessary to avoid error trigger. The banking time is reset once Vsw rises above 2.5V.

Output Voltage Detection

The JW7726BH has output voltage detection function via VO pin. VCC is charged from VO pin when VO is higher than 4.65V to save power loss caused by the LDO when charging from SW pin to VCC pin. When VO drops below 4.55V, the JW7726BH is powered from SW pin.

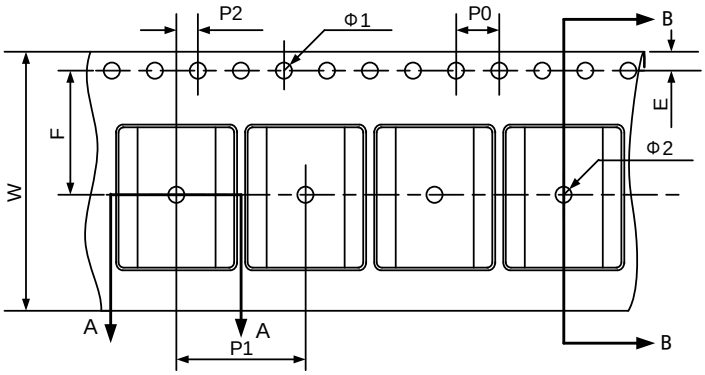
TAPE AND REEL INFORMATION

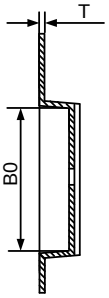
Reel UNIT: mm



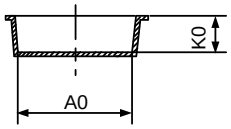
Package	Diameter Φ	Thickness W1	Width W2	W4
SOT23-6	178±2	12.30±2	9.5±2	58±4

Carrier Tape UNIT: mm





SECTION B-B



SECTION A-A

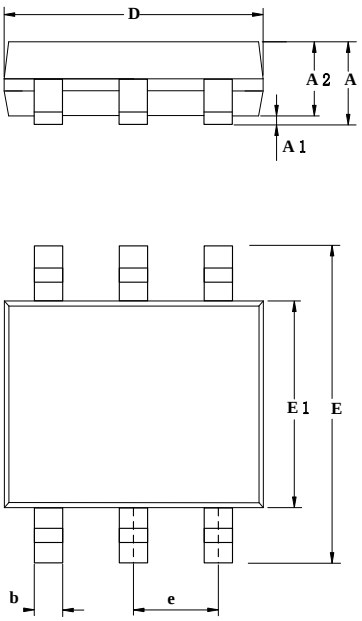
Note :

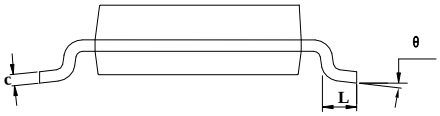
1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

Package	Tape dimensions (mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
SOT23-6	4.0±0.1	2.0±0.1	4.0±0.1	3.23±0.2	3.13±0.3	8.0±0.3	0.25±0.2	1.37±0.2	1.55±0.15	1.00min	1.75±0.1	3.50±0.1

PACKAGE OUTLINE

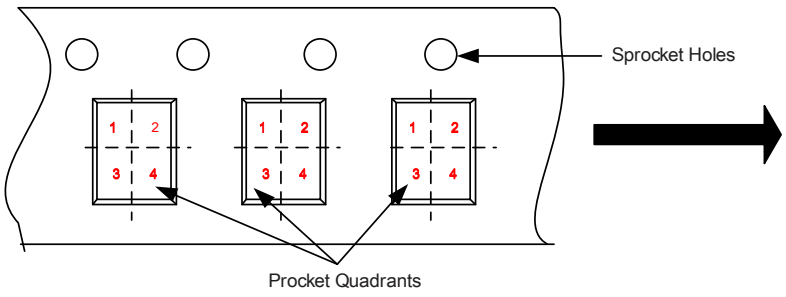
SOT23-6 UNIT: mm





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0	0.05	0.15
A2	0.95	1.10	1.20
b	0.20	0.40	0.60
c	0.05	—	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95（BSC)		
L	0.30	0.45	0.60
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
SOT23-6	3

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