JW5126

65V/200mA
Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW®5126 is a monolithic buck switching regulators based on scheme of hysteresis mode. Operating with an input range of 4.5V~65V, JW5126 delivers 200mA of continuous output current with one integrated N-Channel MOSFET and one integrated P-Channel MOSFET. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. In order to achieve high efficiency at no load while maintaining output voltage regulation, JW5126 operates in low quiescent current and low frequency to maintain high efficiency.

JW5126 guarantees robustness with output short protection, thermal protection, current run-away protection and input under voltage lockout.

JW5126 is available in SOT23-6 and DFN2X3-8 package, which provide a compact solution with minimal external components.

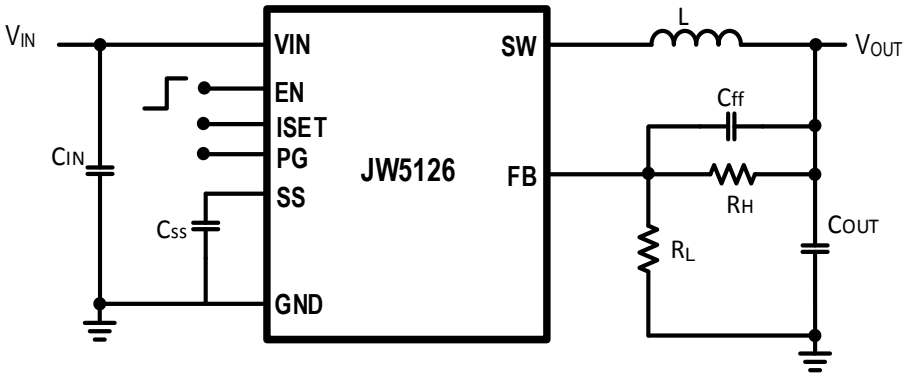
FEATURES

- 4.5V to 65V operating input range
  200mA output current
- Ultra high efficiency at light load
- Adjustable peak current limit
- Internal soft-start (SOT23-6)
- External Soft-start (DFN2X3-8)
- Power Good Indicator (DFN2X3-8)
- Adjustable UVLO and hysteresis
- Current run-away protection
- Output short protection
- Thermal protection
- Available in SOT23-6 and DFN2X3-8 packages

APPLICATIONS

- MCU Supply in Wireless LED Lighting
- Wireless Charger
- Green Electronics/ Appliances
- Point of Load Regulation for High-Performance DSPs
- Industrial and Commercial Low Power Systems

TYPICAL APPLICATION



ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]
JW5126DFNF#TRPBF	DFN2X3-8	JWGU□ YW□□□
JW5126SOTB#TRPBF	SOT23-6	JWGT□ YW□□□

Notes:

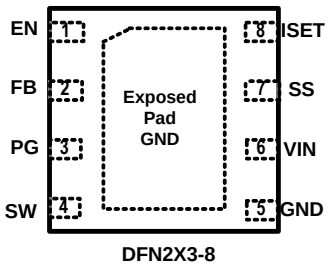
1) JW□□ # TRPBF
- PB Free
- Tape and Reel(If" TR" is not shown, it means tube)
- Package Code
- Part No.

2) Line1: JW□□□
- Internal control code
- Product code
- Joulwatt LOGO

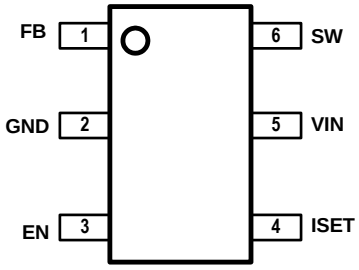
Line2: YW□□□
- Lot number
- Week code
- Year code

PIN CONFIGURATION

TOP VIEW



DFN2X3-8



SOT23-6

ABSOLUTE MAXIMUM RATING[1)]

VIN, SW Pin…….. -0.3V to 72V
SW Pin……..……-0.3V(-5V for 10ns) to 72V(74V for 20ns)
BST Pin..... SW-0.3V to SW+5V
All other Pins ..... -0.3V to 6V
Junction Temperature[2)] 150ºC
Lead Temperature 260ºC
Storage Temperature ..... -65ºC to +150ºC

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN .....4.5V to 65V
Junction Temperature Range .....-40ºC to 125ºC
Ambient Temperature Range .....-40ºC to 85ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
DFN2X3-8	62	7.2ºC/W
SOT23-6	200	130ºC/W

Note:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JW5126 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN=12V, T_A=25℃, Unless otherwise stated。

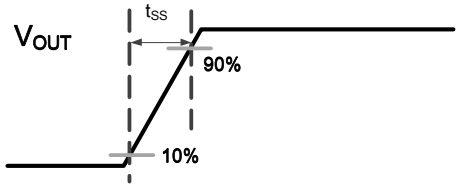
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	4.0	4.2	4.49	V
V_{IN} Under voltage Lockout Hysteresis[5)]	$V_{IN\_MIN\_HYST}$			240		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V			1	μA
Supply Current	I_{Q1}	Active Mode		330	400	μA
	I_{Q2}	Sleep Mode		26	40	μA
Feedback Voltage	V_{FB}		792	800	808	mV
Feedback Pin Current	I_{FB}		-100	0	100	nA
Top Switch Resistance	$R_{DS(ON)T}$			3.5		Ω
Bottom Switch Resistance	$R_{DS(ON)B}$			1.3		Ω
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=65V, V_{EN}=0V, V_{SW}=0V			1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=65V, V_{EN}=0V, V_{SW}=65V			8	μA
High-Side Peak Current Limit	I_{LIMIT1}	1MΩ from ISET to GND		340		mA
		ISET Floating	200	235	270	mA
		500kΩ from ISET to GND	112	140	170	mA
		ISET short to GND	40	50	60	mA
Peak Current Comparator Propagation Delay Time[5)]	$T_{\_delay}$			48		ns
Low-side Current Limit	I_{LIMIT2}	1MΩ from ISET to GND		134		mA
Top Switch Minimum On Time[5)]	T_{ON_MIN}			115		ns
EN Rising Threshold	V_{EN_H}	V_{EN} rising	1.1	1.2	1.3	V
EN Falling Threshold	V_{EN_L}	V_{EN} falling	1.0	1.1	1.2	V
EN Hysteresis	V_{EN_HYS}	V_{EN} Hysteresis		100		mV
Soft-Start Period[5) 6)]	t_{SS}	SS floating		0.65		ms
Soft-Start Charging Current	I_{SS}	V_{SS} = 1 V @DFN2X3-8		2.5		uA
Power Good Threshold - Rising	PG_High	VFB Rising (% of FB voltage) @DFN2X3-8		91		%
Power Good Threshold - Falling	PG_Low	VFB Falling		87		%

VIN=12V, T_A=25℃, Unless otherwise stated。						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
		(% of FB voltage) @DFN2X3-8				
Power Good Delay Time[5)]	PGD_{DLY}	Low to high @DFN2X3-8		340		us
		High to low @DFN2X3-8		13		us
Power Good Sink Current	I_{PG}	PG=0.5V @DFN2X3-8	3			mA
Thermal Shutdown[5)]	T_{TSD}			150		°C
Thermal Shutdown Hysteresis[5)]	T_{TSD_HYST}			20		°C

Note：

5) Guaranteed by design.

6) Soft-Start Period is tested from 10% to 90% of the steady state output voltage.

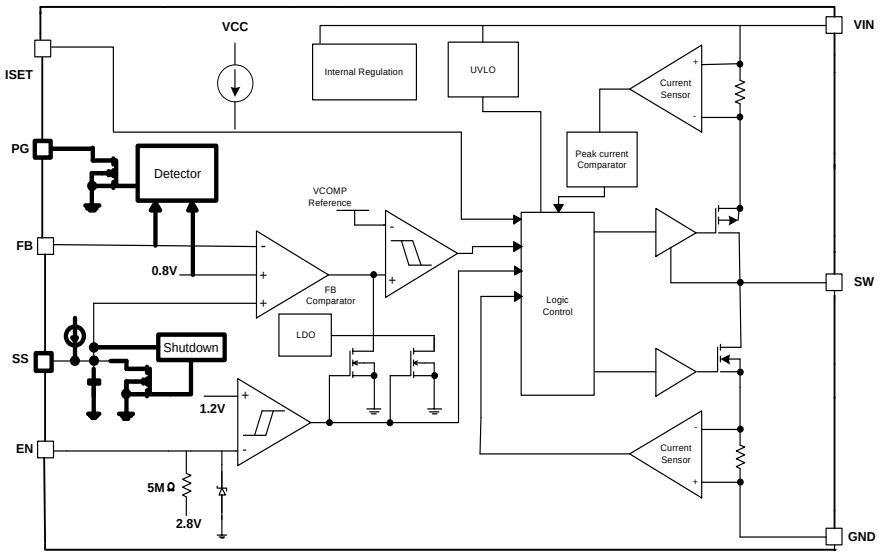


t_{SS} Waveform

PIN DESCRIPTION

DFN2X3-8	SOT23-6	Name	Description
1	3	EN	Enable Control Input. Drive EN pin high or floating to turn on the regulator and low to turn off the regulator.
2	1	FB	Output feedback pin. Connect a resistive divider at FB.
3		PG	Power good open drain output. Asserts low if output voltage is low due to OTP, UVP, UVLO, EN shutdown or during soft-start.
4	6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
5	2	GND	Power ground.
6	5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 65V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
7		SS	Soft-start control pin. Leave floating for internal soft-start slew rate. Connect to a capacitor to extend soft start time.
8	4	ISET	High-side peak current set pin. A resistor from this pin to GND sets the high-side peak current limit. Leave floating for 235mA. Connect 500kΩ resistance for the maximum peak current 140mA. Short this pin to GND for the minimum peak current, 50mA. Connect 1MΩ resistance for the maximum peak current 340mA and low side valley current 134mA.
Exposed Pad		GND	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

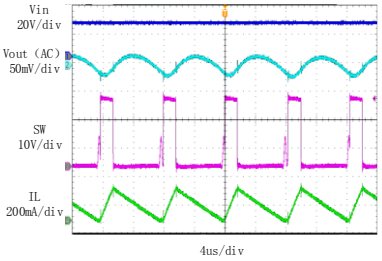
BLOCK DIAGRAM



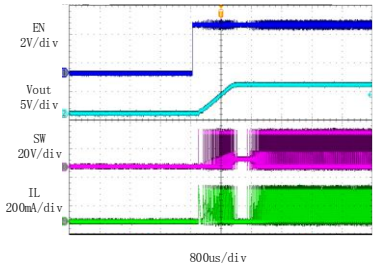
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =24V, V_{OUT}= 5V, L = 150μH, C_{OUT} = 10μF,ISEL=Floating, T_A = +25°C, unless otherwise noted

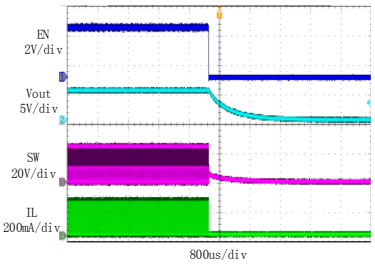
Steady State Test
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.1A



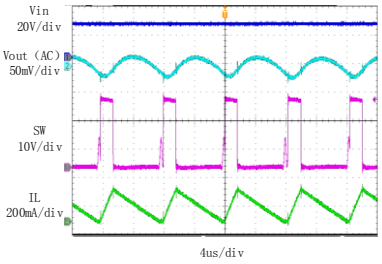
Startup through Enable
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.1A (Resistive load)



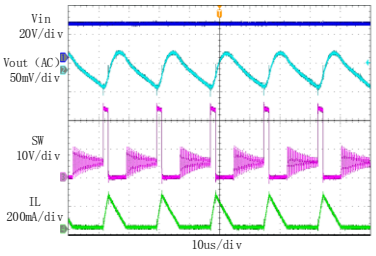
Shutdown through Enable
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.1A (Resistive load)



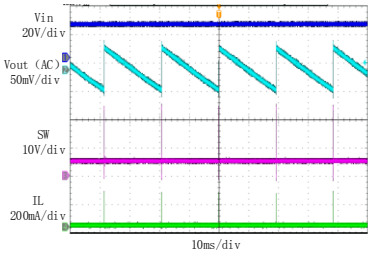
Heavy Load Operation
0.1A LOAD



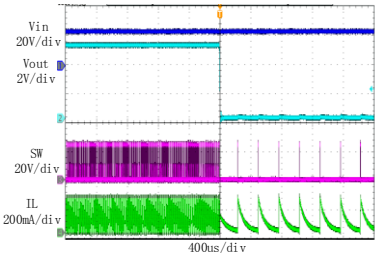
Light Load Operation
0.05A LOAD



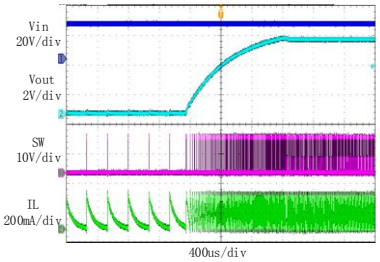
No Load Operation
0 A LOAD



Short Circuit Protection
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.1A- Short

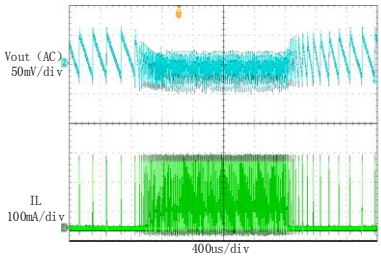


Short Circuit Recovery
V_{IN}=24V, V_{OUT}=5V
I_{OUT}= Short-0.1A



Load Transient
0A LOAD → 0.1A LOAD → 0A LOAD

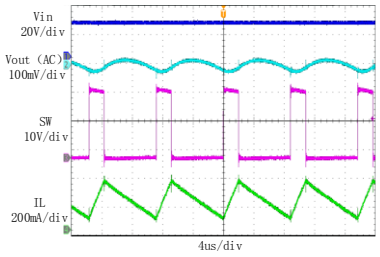
Cff=150pF



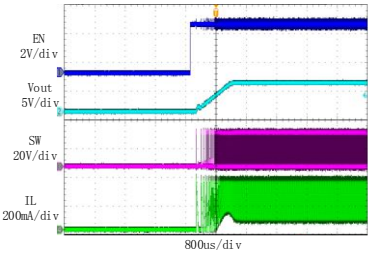
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} =24V, V_{OUT}= 5V, L = 150μH, C_{OUT} = 10μF,ISEL= 1MΩ, T_A = +25°C, unless otherwise noted

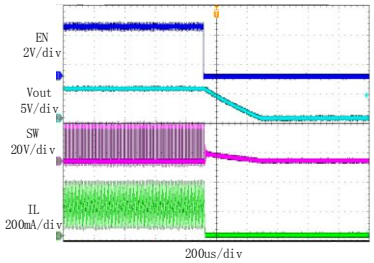
Steady State Test
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.2A



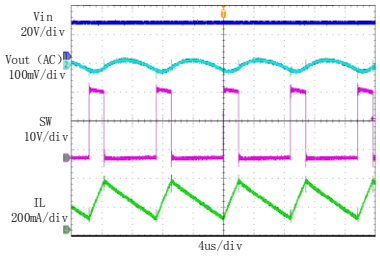
Startup through Enable
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.2A (Resistive load)



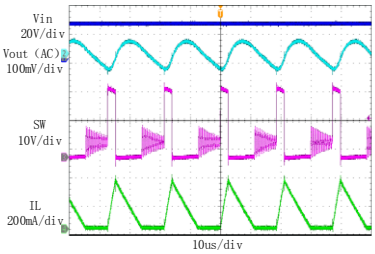
Shutdown through Enable
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.2A (Resistive load)



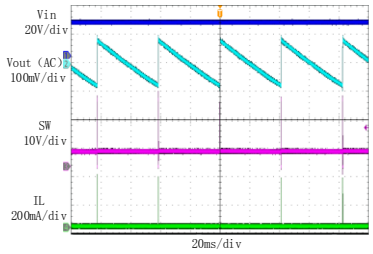
Heavy Load Operation
0.2A LOAD



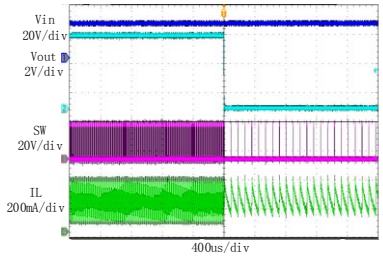
Light Load Operation
0.1A LOAD



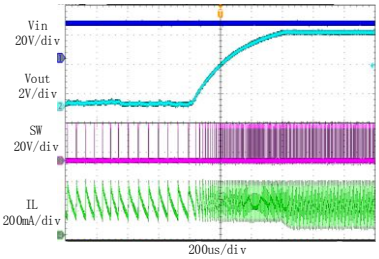
No Load Operation
0 A LOAD



Short Circuit Protection
V_{IN}=24V, V_{OUT}=5V
I_{OUT}=0.2A- Short

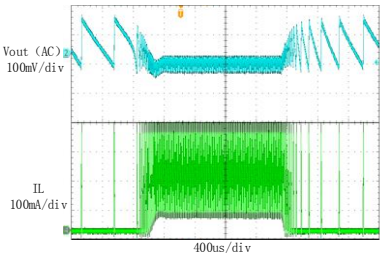


Short Circuit Recovery
V_{IN}=24V, V_{OUT}=5V
I_{OUT}= Short-0.2A



Load Transient
0A LOAD → 0.2A LOAD → 0A LOAD

Cff=150pF



TYPICAL PERFORMANCE CHARACTERISTICS

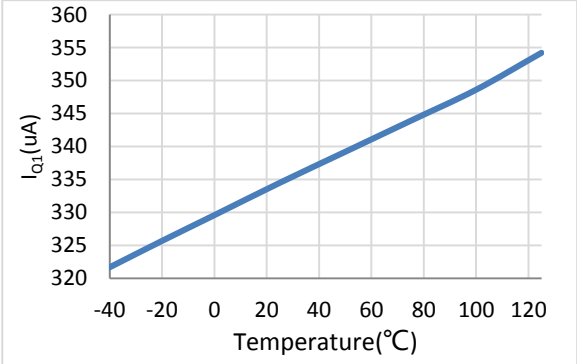


Figure 1. I_{Q1} vs Junction Temperature

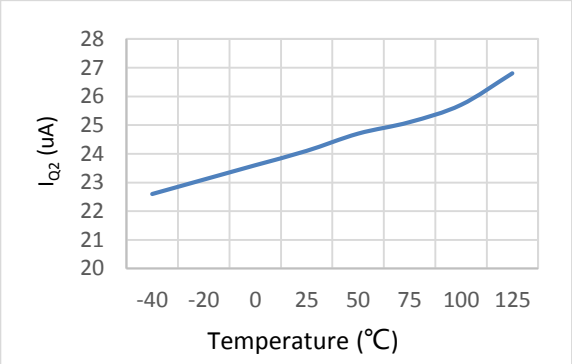


Figure 2. I_{Q2} vs Junction Temperature

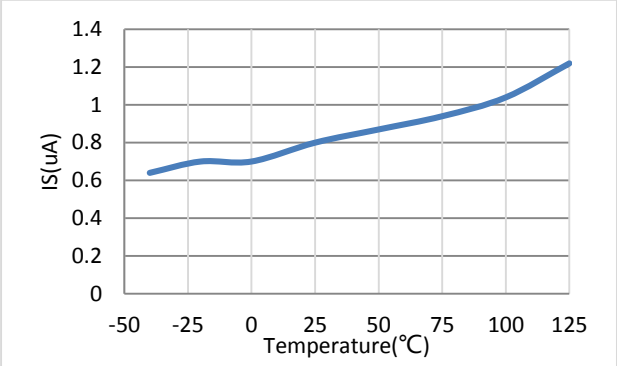


Figure 3. Shutdown Current vs Junction Temperature

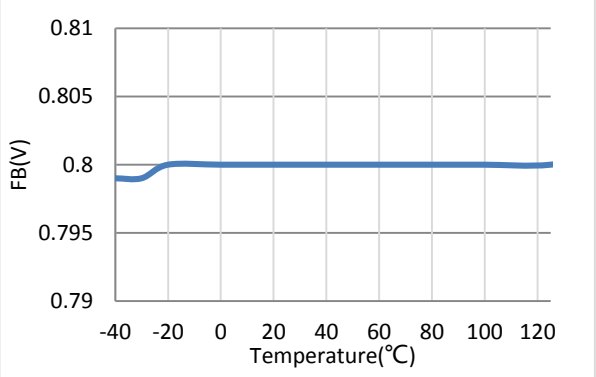


Figure 4. FB Voltage Regulaion vs Junction Temperature

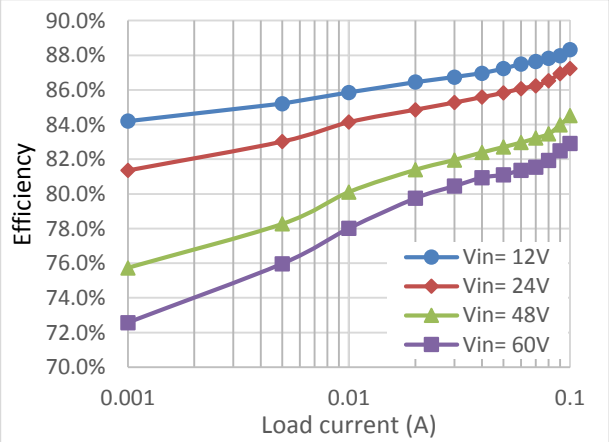


Figure 5. Efficiency vs Load Current

(V_{OUT}=5V, L=150μH)

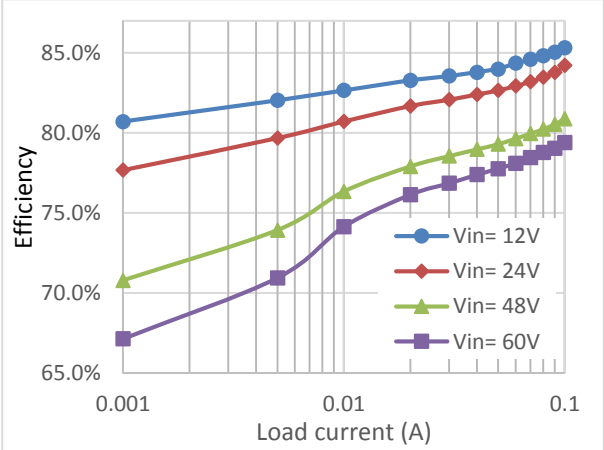


Figure 6. Efficiency vs Load Current

(V_{OUT} =3.3V, L=150μH)

TYPICAL PERFORMANCE CHARACTERISTICS

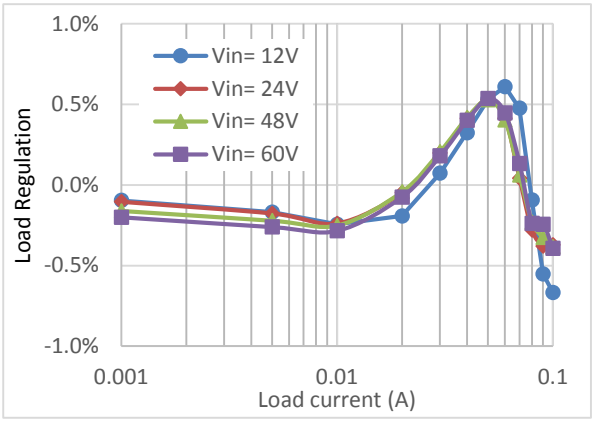


Figure 7. Load Regulation vs Load Current

(V_{OUT} =5V, L=150μH)

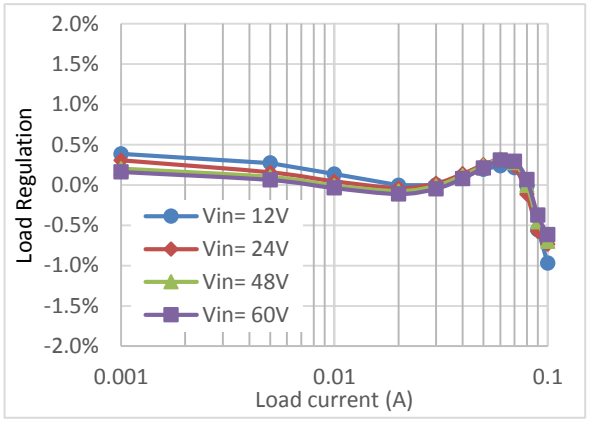


Figure 8. Load Regulation vs Load Current

(V_{OUT} =3.3V, L=150μH)

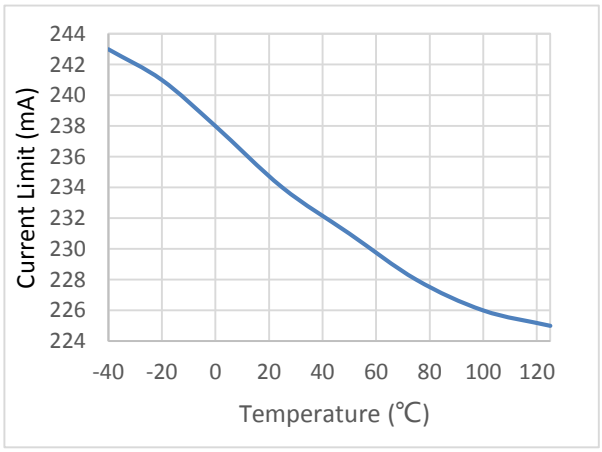


Figure 9. High-Side Peak Current Limit vs Junction Temperature@ Rlimit=Floating

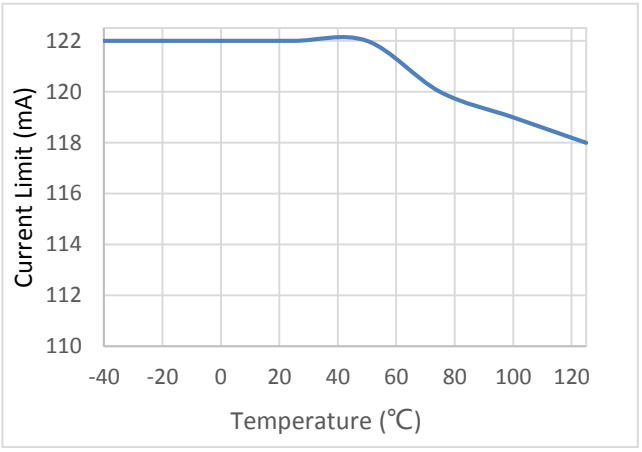


Figure 10. Low-Side Current Limit vs Junction Temperature @Rlimit=1MHz

FUNCTIONAL DESCRIPTION

JW5126 is a synchronous step-down regulator based on scheme of hysteresis mode. It regulates input voltages from 4.5V to 65V down to an output voltage as low as 0.8V, and is capable of supplying up to 200mA of load current.

Scheme of Hysteresis Mode

After comparing the FB voltage with the internal reference voltage 0.8V, the voltage VCOMP can be obtained by integrating the error amplifier. Comparing VCOMP to an internal 1V reference, as shown in Figure11. If this voltage is greater than the reference, the comparator activates a sleep mode in which the power switches and current comparators are disabled, reducing the VIN pin supply current to only 26μA. As the load current discharges the output capacitor, the VCOMP decreases. When this voltage falls 5mV below the 1V reference, the feedback comparator trips. The internal high-side power switch (P-channel MOSFET) is turned on and the inductor current begins to ramp up.

The inductor current increases until either the current exceeds the peak current comparator threshold, or the ON time of the high-side MOSFET exceeds 5μs during the time VCOMP is higher than 1V, at which the high-side power switch is turned off, and the Low-side power switch is turned on.

When 0Ω<=R_{ISET}<=649KΩ or R_{ISET} =floating，the inductor current ramps down until the reverse current is close to zero. If the VCOMP is still less than the 1V reference, the high-side power switch is turned on again and another cycle commences which keep the inductor current operated in a boundary conduction mode. The average current during the BCM will normally be greater than the average load current. For this architecture, the maximum average output current is equal to half of the peak current. The hysteresis nature of this control architecture results in a switching frequency that is a function of the input voltage, output voltage and inductor value.

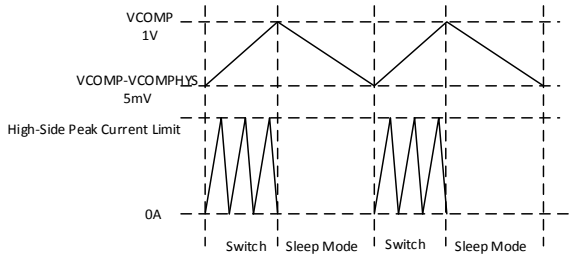


Figure11. Scheme of Hysteresis Mode

When a 1MΩ (820K~1.2M) from ISET to GND, the JW5126 operating in CCM at I_{OUT} larger than 1/2*ILIMIT1, as shown in Figure12. The inductor current increases until either the current exceeds the peak current comparator threshold, or the ON time of the high-side MOSFET exceeds 5μs during the time VCOMP is higher than 1V, at which the high-side power switch is turned off, and the Low-side power switch is turned on. The inductor current ramps down until the inductance current is lower than V_{COMP}*Gcs. Then the high-side switch is turned on.

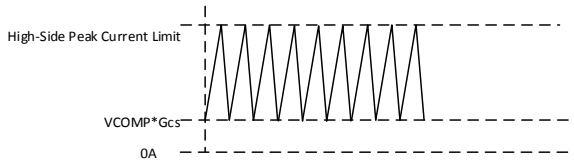


Figure12. CCM Mode

Shut-Down Mode

The regulator shuts down when voltage at EN pin is driven below 0.3V. The entire regulator is

off and the supply current consumed by the regulator drops below 1μA.

Enable and Adjustable UVLO Protection

The JW5126 is enabled when the VIN pin voltage rises above 4.2V and the EN pin voltage exceeds the enable threshold of 1.2V. The JW5126 is disabled when the VIN pin voltage falls below 3.9V or when the EN pin voltage is below 1.1V. The EN pin has an internal pull-up resistor that enables operation of the JW5126 when the EN pin floats.

If an application requires a higher VIN under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 13). So that when VIN rises to the pre-set value, EN rises above 1.2V to enable the device and when V_{IN} drops below the pre-set value, EN drops below 1.1V to trigger input under voltage lockout protection.

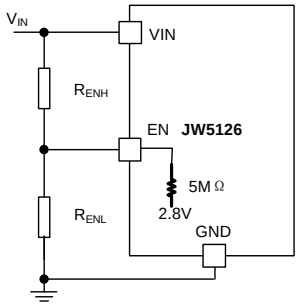


Figure13. Adjustable UVLO

The input voltage UVLO threshold (V_{UVLO}) and hysteresis (V_{UVLO_HYS}) can be calculated by the following equation.

$$V_{UVLO} = \left(V_{EN\_H} - \frac{2.8V}{5M\Omega * \frac{R_{ENH} + R_{ENL}}{R_{ENH} * R_{ENL}} + 1} \right) * \left(R_{ENH} * \frac{5M\Omega + R_{ENL}}{5M\Omega * R_{ENL}} + 1 \right)$$

$$V_{UVLO\_HYS} = \left(R_{ENH} * \frac{5M\Omega + R_{ENL}}{5M\Omega * R_{ENL}} + 1 \right) * V_{EN\_HYS}$$

When R_{ENL} <=100KΩ, V_{UVLO} can be calculated approximately according to the following equation.

$$V_{UVLO} = \frac{R_{ENH} + R_{ENL}}{R_{UVLO\_lower}} * V_{EN\_H}$$

$$V_{UVLO\_HYS} = \frac{R_{ENH} + R_{ENL}}{R_{ENL}} * V_{EN\_HYS}$$

where

V_{EN_H} is enable shutdown threshold (1.2V typ.);

V_{EN_HYS} is enable shutdown hysteresis (100mV typ.);

Output Short Protection

JW5126 inherent short−circuit protection. If the output is shorted to ground, the inductor current will decay very slowly during a single switching cycle. Since the high-side switch turns on only when the inductor current is near zero at 0Ω <=R_{ISET}<=649KΩ or R_{ISET} =floating, or near 134mA at R_{ISET} =1MΩ (820K~1.2M), the JW5126 inherently switches at a lower frequency during short-circuit condition.

External Soft-start

(DFN2X3-8)

Soft-start is designed in DFN2X3-8 package to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 2.5uA is designed to charge the external soft-start capacitor (C_{SS}). When it is less than internal reference voltage (V_{REF}, typ. 0.8V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

The soft start time T_{SS} can be calculated by the following equation.

$$T_{SS}(ms) = \frac{0.8 * C_{SS}(nF) * V_{REF}(V)}{I_{SS}(uA)}$$

Power Good

(DFN2X3-8)

The DFN2X3-8 package has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to a voltage source (such as V_{OUT}) through a resistor. When the FB voltage exceeds 91% of the internal reference V_{REF}, the internal PG switch turns off and PG can be pulled high by the external pull-up. If the FB voltage falls below 87% of V_{REF}, the internal PG switch turns on, and PG is pulled low to indicate that the output voltage is out of regulation. The rising edge of PG has a built-in deglitch delay of 340 µs.

Thermal Protection

When the temperature of the regulator rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 130°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

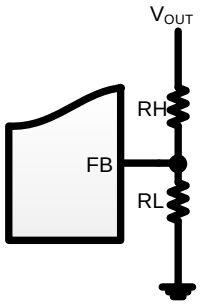
The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

If R_L is determined, and then R_H can be calculated by:

$$R_H = R_L * \left(\frac{V_{OUT}}{0.8} - 1\right)$$



High-Side Peak Current Limit

The peak current can be programmed from 50mA to 236mA by changing the resistor between ISET pin and ground. The peak current setting resistor RISET can be calculated by the formula:

When 0Ω<=R_{ISET}<=649KΩ

$$I_{LIMIT1}\ (mA)\ = 0.18 * R_{ISET}\ (K\Omega)\ + 50$$

When R_{ISET} =floating

$$I_{LIMIT1}(mA) = 225mA$$

When 820KΩ<=R_{ISET}<=1200KΩ

$$I_{LIMIT1}\ (mA)\ = 0.167 * R_{ISET}\ (K\Omega)\ + 193$$

When 0Ω<=R_{ISET}<=649KΩ or R_{ISET} =floating setting I_{LIMT1}, be noticed that the maximum output current is equal to half of the I_{LIMT1}. Make sure the I_{LIMT1} is high enough for the output current requirement. Also be noticed that higher I_{LIMT1} would result in higher inductor current ripple, larger input and output voltage ripple, which means bigger components (inductor, input and output capacitors).

When 820KΩ<=R_{ISET}<=1200KΩ，the maximum output current is equal to 1/2*(I_{LIMT1}+ I_{LIMT2}), where I_{LIMT2} is low side current limit （I_{LIMT2}=134mA）.

Output Capacitor

The output capacitor, C_{OUT}, filters the inductor's ripple current and stores energy to satisfy the load current. when the JW5126 is in sleep mode. The value of the output capacitor must be large enough to accept the energy stored in the inductor without a large change in output voltage. To achieve an output voltage peak-peak ripple less than 1% of the output voltage, the output capacitor must be:

$$C_{OUT} \geq 50 * L * \left(\frac{I_{LIMIT1}}{V_{OUT}}\right)^2 * \frac{V_{IN}}{V_{IN} - V_{OUT}}$$

Inductor

As the I_{LIMT1} is determined, for given input voltage and output voltage, the inductor value can be determined by the following formula:

$$L = \frac{V_{OUT}}{f_{SW} * I_{LIMIT1}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{sw} is the switching frequency at the maximal output current, and I_{LIMIT1} is the high side peak current.

Larger inductor value results in lower switching frequency, as well as higher efficiency. However, the larger value inductor will have a larger physical size, higher series resistance, and lower saturation current as well as the slow load

transient dynamic performance. There is also a lower limit of the inductor value, which is determined by the minimum on time. In order to keep the inductor working under control, the inductor value should be chosen higher than L_{MIN} that is derived from below formula:

$$L_{MIN} = \frac{V_{IN\_MAX} * T_{ON\_MIN}}{I_{LIMIT1}}$$

Where VIN_MAX is the max value of input voltage. TON_MIN is the designed 110ns minimum switch on time.

Switch Frequency

Switching frequency can be estimated by below equation.

$$f_{sw} = \frac{2 * I_{OUT} * V_{OUT} * (V_{IN} - V_{OUT})}{{I_{LIMIT1}}^2 * V_{IN} * L}$$

Higher I_{LIMIT1} and inductor can get lower fsw. And fsw increases as I_{OUT} increasing. When I_{OUT} increases to $I_{LIMIT1}/2$, fsw also reaches its highest value and can be derived by:

$$f_{sw\_MAX} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{I_{LIMIT1} * V_{IN} * L}$$

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5126 (VIN pin and GND pin) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. Keep the switching node SW short to prevent excessive capacitive coupling
4. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

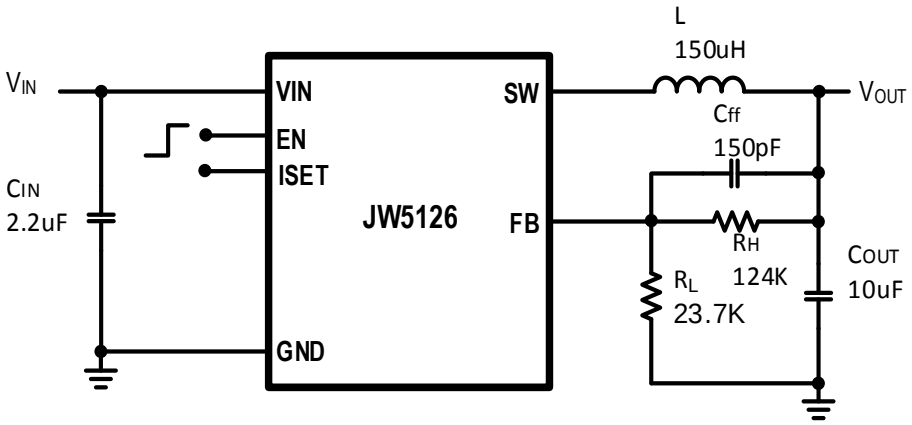
REFERENCE DESIGN For SOT23-6

Reference 1:

V_{IN}: 6V~60V

V_{OUT}: 5V

I_{OUT}: 0~0.1A

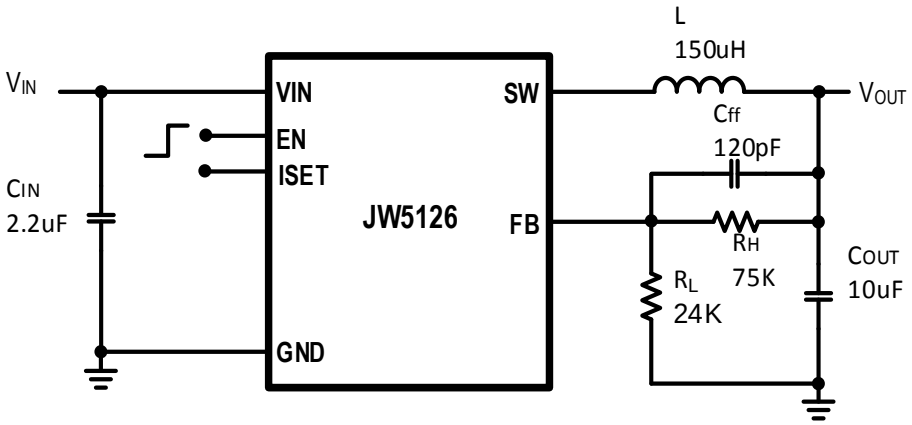


Reference 2:

V_{IN}: 4.5V~60V

V_{OUT}: 3.3V

I_{OUT}: 0~0.1A

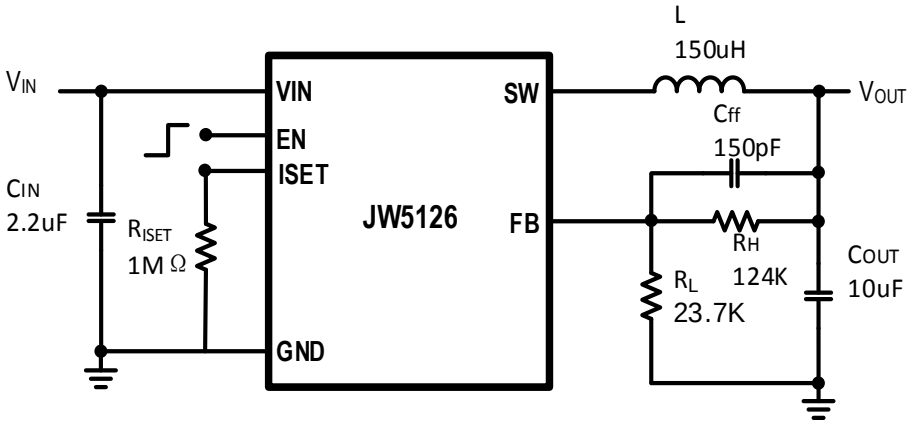


Reference 3:

V_{IN}: 6V~60V

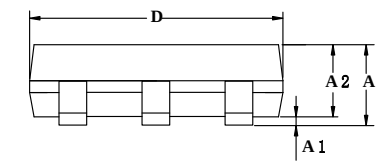
V_{OUT}: 5V

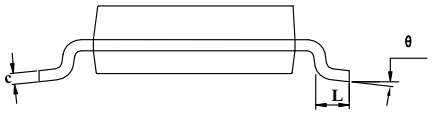
I_{OUT}: 0~0.2A

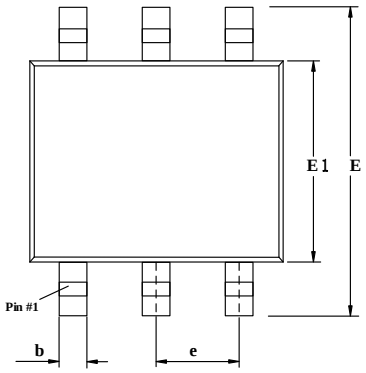


PACKAGE OUTLINE

SOT23-6 UNIT: mm

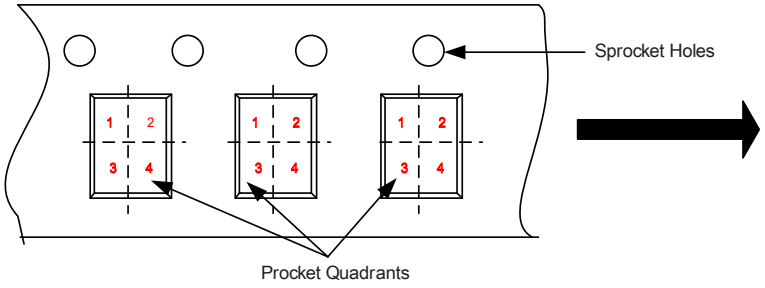






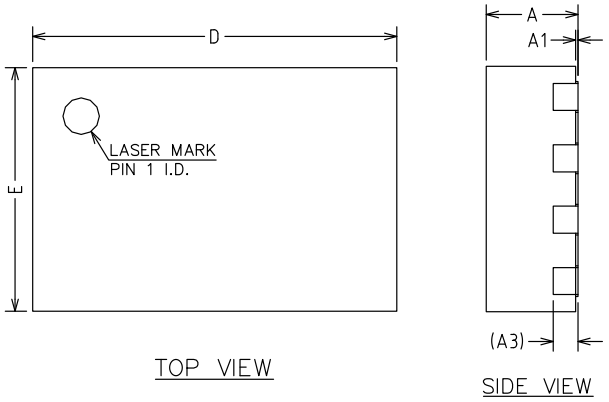
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0	0.05	0.15
A2	0.95	1.10	1.20
b	0.20	0.40	0.60
c	0.05	—	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95（BSC）		
L	0.30	0.45	0.60
θ	0°	—	8°

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
SOT23-6	3

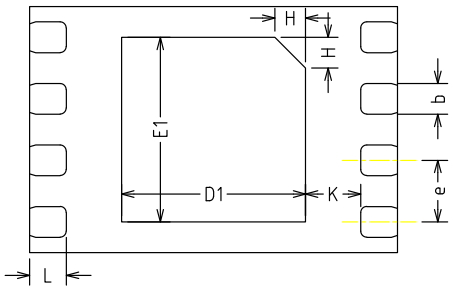
DFN2x3-8 UNIT: mm



TOP VIEW

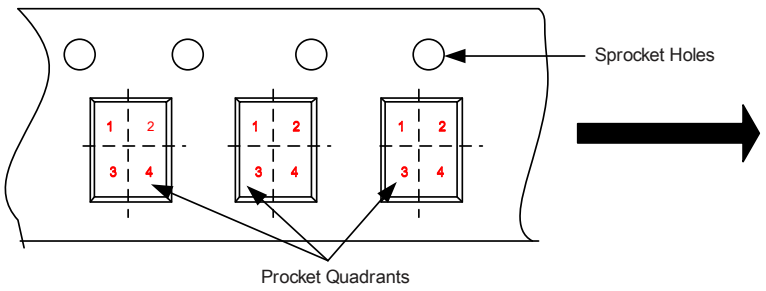
SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	2.93	3.00	3.07
E	1.93	2.00	2.07
D1	1.40	1.50	1.60
E1	1.40	1.50	1.60
e	0.40	0.50	0.60
H		0.20 REF	
K	0.20	—	—
L	0.23	0.30	0.37



BOTTOM VIEW

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
DFN2X3-8	2

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