

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW[®]3902 is a highly integrated synchronous switch mode boost charger for 2 or 3 cells Li-ion or Li-polymer applications. It integrates battery balance for 2 cells E-cigarette application. It can charge the battery from an input range 3.6V to 5.5V, the input break down voltage is up to 20V.

The JW3902 supports I²C serial communication interface to program charge current up to 3.15A and program charge voltage up to 13.05V for different portable applications. It also has a programmable charge timeout for safety battery charge operation and a programmable input voltage threshold for adaptive input current limit. Pre-charge current and charge termination current can also be programmed through I²C interface.

The JW3902 guarantees robustness with adaptive input current limit, input over-voltage protection, battery under-voltage and over voltage protection, charging timeout, battery temperature protection, watchdog timeout and thermal shutdown.

The JW3902 is available in QFN4x4-24 package.

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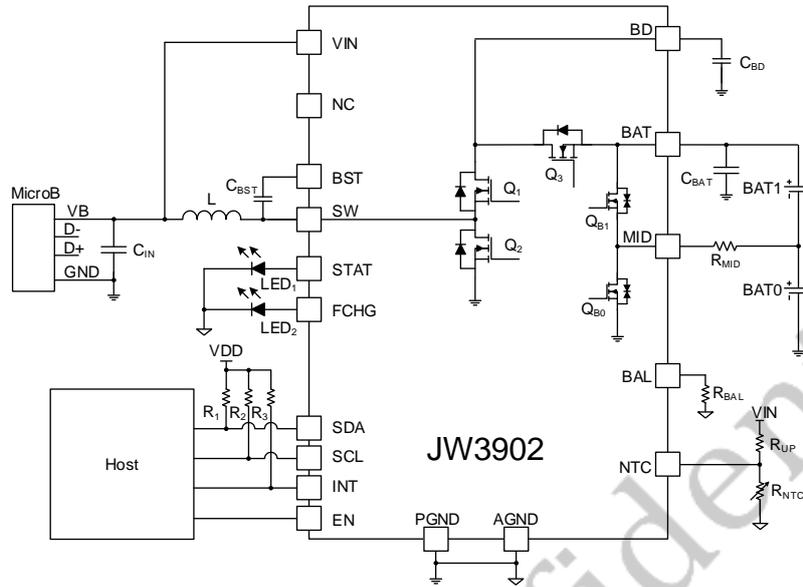
FEATURES

- Integrate Synchronous Boost Charger
- Up to 20V Breakdown Voltage
- 3.6V to 5.5V Input Voltage Range
- Support 2-3 Cells Battery Charge
- Cell Balance Function for 2 Cells
- Charge Parameter can be Programmed through I²C Interface
 - Charge Current
 - Charge Voltage
 - Charge Timer
 - Adaptive Input Current Limit
 - Pre-Charge Current and Charge Termination current
- Charge Status Indication
- Safety
 - Input Over-Voltage Protection
 - Battery Under Voltage and Over-Voltage Protection
 - Battery Temperature Protection
 - Charging Timeout
 - Watchdog Timeout
 - Thermal Shutdown
- Ultra-Low Quiescent Current: <1uA
- Package: QFN4x4-24

APPLICATIONS

- E-Cigarette
- Blue Tooth Speaker Charger
- E-Joy
- POS Machine

TYPICAL APPLICATION



ORDER INFORMATION

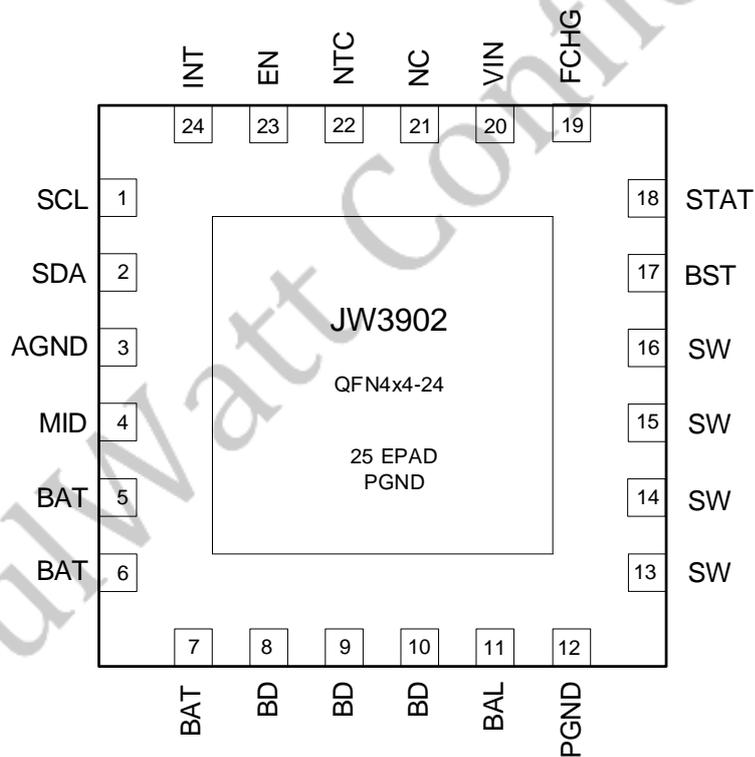
DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW3902QFN#TRPBF	QFN4x4-24	JW3902 YW□□□□

Note:



PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING¹⁾

VIN, SW, BD, BAT, MID, EN, NTC, STAT, FCHG.....	-0.3V to 20V
BST-SW.....	-0.3V to 7V
INT, SCL, SDA, BAL.....	-0.3V to 7V
Junction Temperature ²⁾³⁾ (T _J (MAX)).....	-40°C to 150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS⁴⁾

Input Voltage VIN	3.6V to 5.5V
Battery Voltage VBAT	0V to 13.5V
Charge Current.....	0A to 3.15A
Operation Junction Temp (T _J)	-40°C to +125°C

THERMAL PERFORMANCE⁵⁾

	θ_{JA}	θ_{JC}
QFN4x4-24.....	48	3.5°C/W

Note:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATIONF CONDITIONS
- 2) The JW3902 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The maximum allowable continuous power dissipation at any ambient temperature is calculated by $PD (MAX) = (T_J(MAX)-T_A)/\theta_{JA}$.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN}=5V$, $V_{BAT}=7.4V$, $T_J=-40^{\circ}C$ to $125^{\circ}C$ and $T_J=25^{\circ}C$ for typical values (unless otherwise stated)

Item	Symbol	Condition	Min.	Typ.	Max.	Units
Charge mode						
Input voltage	V_{IN}		3.6		5.5	V
VIN under-voltage lock-out threshold	V_{IN_UVLO}	V_{IN} rising		3.65		V
		V_{IN} falling		3.55		V
VBAT under-voltage lockout threshold	V_{BAT_UVLO}	V_{BAT} rising		3.65		V
		V_{BAT} falling		3.55		V
Quiescent current into BAT pin	I_{Q_BAT}	EN=L, $V_{IN}=0V$, $V_{BAT}=8V$		0.6		uA
Input voltage limit threshold	V_{INDPM}	VINDPM=4.4V(011b), programmed by I2C		4.4		V
Charge current in CC charge phase	I_{CHG}	ICHG=1A(010100b), programmed by I2C		1.0		A
		ICHG=100mA(000010b), programmed by I2C		100		mA
Battery voltage regulation target	V_{CV}	BATCV=8.15V(000b)		8.15		V
		BATCV=8.4V(001b)		8.4		V
		BATCV=8.5V(010b)		8.5		V
		BATCV=8.7V(011b)		8.7		V
		BATCV=12.23V(100b)		12.23		V
		BATCV=12.6V(101b)		12.6		V
		BATCV=12.75V(110b)		12.75		V
		BATCV=13.05V(111b)		13.05		V
Battery full charge enable threshold	V_{FULL}			97		% V_{CV}
Battery recharge threshold	V_{RECHG}	VBAT falling		97		% V_{CV}
Battery full charge deglitch time ⁶⁾	t_{FULL}			500		ms
Charge termination current	I_{TERM}	ITERM=100mA(001b)		100		mA
The step length of charge current increase ⁶⁾	I_{STEP}			50		mA
The step time of charge current increase ⁶⁾	t_{STEP}			2		ms
Trickle mode charge current	I_{TRI}	IPRECHG=100mA(001b)		100		mA
Top MOSFET on-resistance	$R_{DSTG(ON)}$			20		mΩ
Bottom MOSFET on-resistance	$R_{DSBG(ON)}$			40		mΩ
Reverse block MOSFET	$R_{DSRB(ON)}$			30		mΩ

on-resistance						
Switch frequency	f_{SW}	FSW=500kHz(00b)		500		kHz
		FSW=750kHz(01b)		750		
		FSW=1MHz(10b)		1000		
		FSW=1.5MHz(11b)		1500		
Trickle mode battery threshold	V_{TRI}	$V_{IN}=5V, V_{CV}<9V, 2$ cells, V_{BAT} rising		5.6		V
		$V_{IN}=5V, V_{CV}<9V, 2$ cells, V_{BAT} falling		5.5		V
		$V_{BAT}=5V, V_{CV}>9V, 3$ cells, V_{BAT} rising		8.4		V
		$V_{BAT}=5V, V_{CV}>9V, 3$ cells, V_{BAT} falling		8.3		V
Thermal regulate threshold ⁶⁾	T_{REG}	TREG_SEL=0b		130		°C
		TREG_SEL=1b		145		°C
Maximum sink current on STAT pin and FCHG pin	I_{SINK}			5		mA
Battery Balance						
The Discharge MOS On Resistance	R_{BAL}			8		Ω
Cell balance start voltage	V_{BALST}	BAL_START=3.7V(0b)		3.7		V
		BAL_START=4.05V(1b)		4.05		V
Balance Threshold	ΔV_{CELL}	BAL_DIFF=30mV(0b)		30		mV
		BAL_DIFF=40mV(0b)		40		mV
Balance time ⁶⁾	t_{BAL}			1		s
Charging stop voltage during battery balance	$V_{CHGSTOP}$	BAL_CHGSTOP=4.1V(00b)		4.1		V
Protection						
VIN Over voltage threshold	V_{IN_OVP}	VIN rising		6.5		V
		VIN falling		6.2		
NTC under temperature threshold	NTC_L	NTCL_SEL [1:0] = 01b 0°C		73.2%		V_{IN}
		Recovery 5°C		68.8%		
		NTCL_SEL [1:0] = 10b -5°C		77.2%		
		Recovery 0°C		73.2%		
		NTCL_SEL [1:0] = 11b -10°C		80.9%		
		Recovery -5°C		77.2%		
NTC over temperature threshold	NTC_H	NTCH_SEL [1:0] = 01b 45°C		32.9%		V_{IN}
		Recovery 40°C		36.8%		
		NTCH_SEL [1:0] = 10b 55°C		26.1%		

		Recovery50°C		29.4%		
		NTCH_SEL [1:0] = 11b 60°C		23.2%		
		Recovery55°C		26.1%		
Charge time-out period ⁶⁾	t _{CHG}	CHG_TIMER=00b (Disable) Default		∞		h
		CHG_TIMER=01b		6		
		CHG_TIMER=10b		12		
		CHG_TIMER=11b		24		
Charge time-out period in trickle mode ⁶⁾	t _{CHG_TC}			20%		t _{CHG}
Thermal shutdown threshold	T _{SHUT}			T _{REG} +20		°C
Over temperature hysteresis	T _{OT_HYS}			20		°C
Watchdog time-out period ⁶⁾	t _{WD}			20		s
Battery under-voltage threshold to disable battery balance	V _{BAT_UVP}	VBAT falling, BAL_SEL=10b		3.0		V
Battery over voltage threshold	V _{BAT_OVP}	VBAT rising, as percentage of battery voltage regulation target	102	104	106	%V _{CV}
		VBAT falling, as percentage of battery voltage regulation target	100	102	104	%V _{CV}

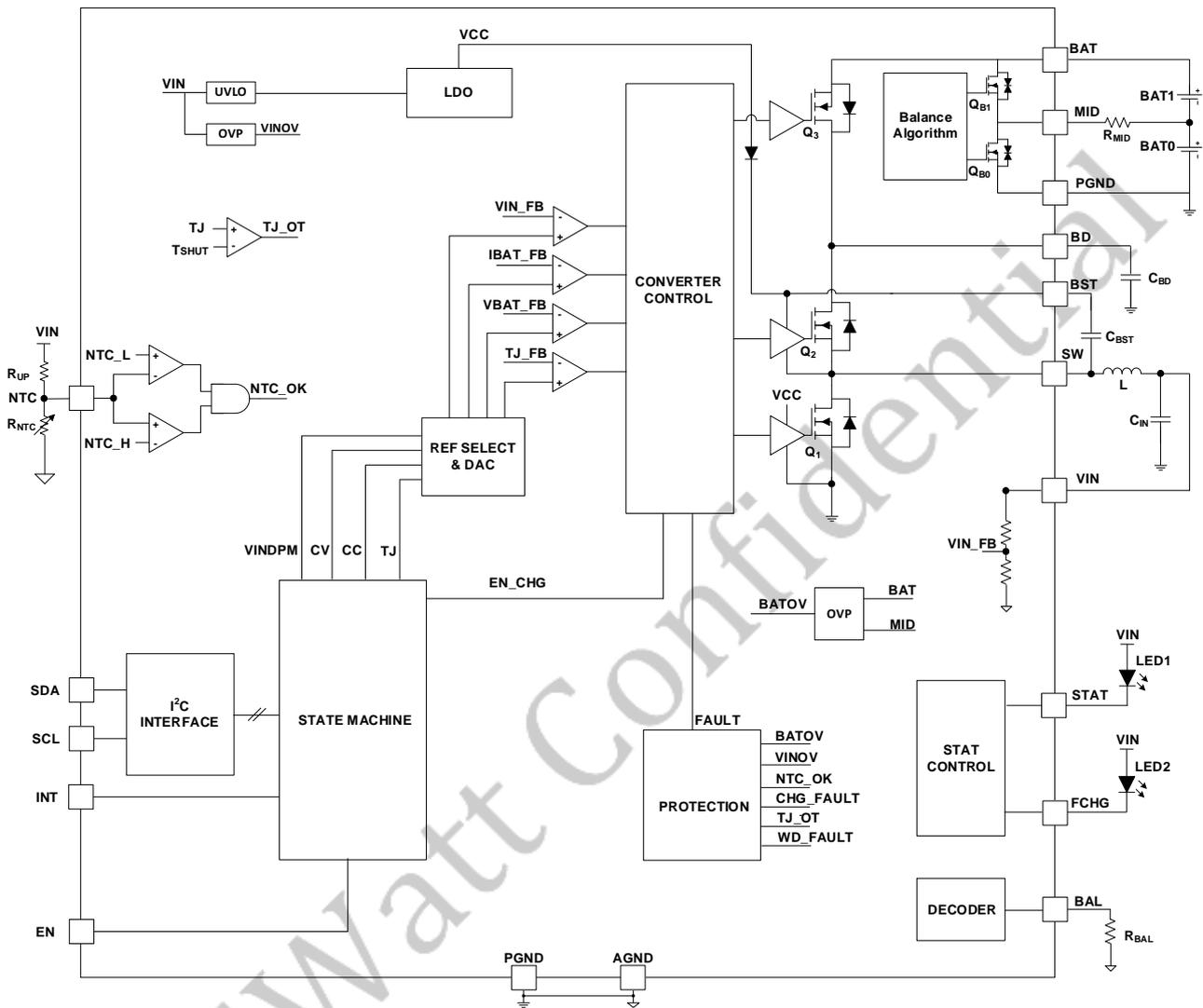
Notes:

6) Guaranteed by design.

PIN DESCRIPTION

Pin No.	Name	Description
1	SCL	I2C interface serial clock pin, logic level input.
2	SDA	I ² C interface serial data pin, logic level input/output.
3	AGND	Analog ground
4	MID	Battery balance pin.
5-7	BAT	Battery input pin, connect to battery positive node to detect the battery voltage
8-10	BD	Boost output pin.
11	BAL	Battery balance setting. Connect a resistor less than 100k from this pin to GND to disable battery balance function. Connect a resistor larger than 150k from this pin to GND to enable battery balance function.
12	PGND	Power ground
13-16	SW	Switching node. Connected to inductor.
17	BST	High side driver positive supply. Internally, the BST pin is connected to the cathode of the boost-strap diode. Connect the 0.1μF bootstrap capacitor from SW to BST.
18	STAT	Charge status pin output. Logic High indicates charge is in progress. Logic Low indicates charge is complete. When charge fault occurs, the stat pin blinks at 1Hz.
19	FCHG	Full charge LED driver.
20	VIN	Input pin.
21	NC	No connection.
22	NTC	Temperature qualification voltage input pin.
23	EN	Chip enable pin.
24	INT	Open-drain interrupt output. Connect the INT to a logic rail through 4.7kΩ resistor. The INT pin sends an active LOW, 512μs pulse to host to report charger device status and fault.
25	PGND	Exposed pad, power ground.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

JW3902 is a highly integrated synchronous switch mode boost charger for 2 or 3 cells Li-ion or Li-polymer applications. It integrates battery balance for 2 cells E-cigarette application. It can charge the battery from an input range 3.6V to 5.5V, the input break down voltage is up to 20V. Integrated reverse block MOSFET can disconnect output when output short circuit or shutdown happens. The programmable switching frequency (set by FSW bits in REG02 register) is beneficial to optimization of circuit design and the default frequency is 1MHz.

I²C interface is available for the chip to provide flexible system solutions, through which user can program the charging current, charging voltage, charge timeout, input voltage threshold, pre-charge current, charge termination current and other parameters easily. User can refer to the register map for detailed information.

Operation Status Description

The JW3902 has two open-drain output pins (STAT Pin, FCHG Pin) for describing charge status. Current limit resistors and LEDs from VIN to these pins can realize the above function easily.

When charge is in progress, the STAT pin output LOW and the FCHG output high-impedance state.

When charge is completed or charger is in sleep mode, the STAT pin is output high-impedance state and the FCHG output LOW.

When charge suspend at fault condition, the STAT pin blinks at 1Hz and the FCHG output high-impedance state.

Shutdown mode

The chip is in shutdown mode when the battery is present, EN is pulled low and input voltage V_{IN} is lower than V_{IN_UVLO} . In this mode, the chip stops switching and disables all the modules for minimum quiescent current less than 1uA from the battery.

IDLE mode

The chip enters into IDLE mode when the battery is present and $(EN=H \& V_{IN} < V_{IN_UVLO}) \vee (EN=L \& V_{IN} > V_{IN_UVLO})$. In this mode, the chip stops switching and all modules except I²C, MCU can access registers by I²C.

Charge mode

The chip enters into charge mode when the battery is present, EN is logic high and VIN_PRESENT bit in REG06 register is set to 1. When V_{IN} is higher than V_{IN_UVLO} (3.65V), VIN_PRESENT bit in REG06 register will be set to 1, and the chip outputs an INT interrupt pulse to inform MCU. When VIN_PRESENT=1 and $V_{IN} < V_{IN_OVP}$, the chip sets ACOK bit in REG06 register to 1. IF ACOK=1 and EN_CHG bit in REG04 register is set to 1, the device starts switching and charges the battery on trickle charge, constant current charge, constant voltage charge and charge termination according to the battery voltage. The charge profile is shown in the figure below.

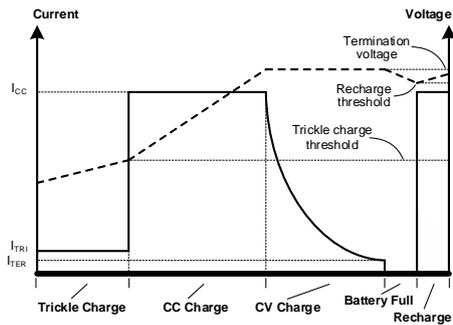


Figure 1. Charge profile

Battery Charging Management

Trickle Charge

When the battery voltage is lower than trickle charge threshold V_{TRI} , the device charges the battery in trickle mode. In this phase, the trickle charging current I_{TRI} is set by IPRECHG bits in REG02 register.

For 2 cells battery application:

$V_{TRI} = \max(5.6V, n \cdot V_{IN})$, $n = 1.1$ when switching frequency $f \leq 1$ MHz and $n = 1.2$ when switching frequency $f > 1$ MHz.

For 3 cells battery application:

$V_{TRI} = \max(8.4V, n \cdot V_{IN})$, $n = 1.1$ when switching frequency $f \leq 1$ MHz and $n = 1.2$ when switching frequency $f > 1$ MHz.

Constant Current (CC) Charge

When the battery voltage is higher than the trickle charge threshold V_{TRI} , the device always charges the battery in constant current charge threshold I_{CC} if the input current is sufficient. When input current limit is hit, the device reduces the charge current automatically. In this phase, the device charges the battery with I_{CC} set by ICHG bits in REG01 register.

Constant Voltage (CV) Charge

When the battery voltage reaches constant voltage charge V_{CV} , the device regulates the battery voltage and reduce the charge current

automatically. In this phase, the battery charge voltage V_{CV} for 2 or 3 cells is set by BATCV bits in REG00 register.

Charge Termination

When battery voltage is higher than $V_{FULL}(97\%V_{CV})$ and the charge current is less than charge termination current I_{TERM} (decided by ITERM bits in REG02 register) for $t_{FULL}(500ms)$, the charge process terminates.

Recharge

When charge process terminates, the battery voltage may drop slowly due the leakage or operation current from the battery. Once the battery voltage drops below 97% of the setting voltage V_{CV} , the chip resumes switching to recharge the battery.

Adaptive Input Current Limit

If the output current of the adapter is limited, it may crash when the current drawn by the charger is higher than its output current capability. The JW3902 supports adaptive input current limit function to solve problem.

The allowed minimum input voltage can be set in VINDPM bits in REG00 register. When the input voltage is pulled down to the setting threshold, due to the limited output current capability of the adapter, the chip reduces the charging current automatically to regulate the input voltage at the setting threshold and prevent the adapter from crashing.

Thermal Regulation Control

The JW3902 integrates temperature loop to avoid chip temperature rising too much. When the junction temperature of the device reaches T_{REG} which is set by THEG_SEL bit in REG04 register, the chip sets THERMAL_STAT bit in

REG06 register to 1 and reduces the charge current in order to prevent further increase in chip temperature.

Soft Start

The JW3902 features soft start function to avoid any current or voltage inrush during the start process.

When the device works in charge mode, it will increase battery charging current from 0 to the setting value with default rate of 50mA/2ms, during the start process, and it decreases battery charging current directly without soft state function.

Similarly, when the following condition occurs, charge current soft starts up to the presetting value.

- 1) Charge-cycle starts up;
- 2) MCU turns up the charge current;
- 3) Charge current turn up from trickle charge to CC charge;
- 4) Charge cycle restarts when faults are removed or recharge occurs.

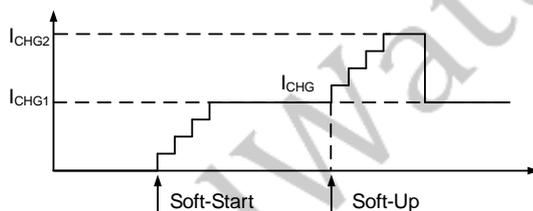


Figure 2. Charge current soft start

Adapter Attachment / Detachment / Over-voltage Indication

When VIN pin is connected to the adapter input port as shown in the typical application circuit, the JW3902 can detect the adapter attachment/detachment/over-voltage event.

When the voltage of VIN pin rises above V_{IN_UVLO} rising threshold, the VIN_PRESENT bit

in REG06 register is set to 1 and the chip outputs an INT interrupt pulse to inform MCU; when the voltage of VIN pin falls below V_{IN_UVLO} falling threshold, the VIN_PRESENT bit is cleared.

When the voltage of VIN pin rises above V_{IN_OVP} rising threshold, the ACOK bit in REG06 register will be cleared, and VIN_OVP bit in REG07 register is set to 1; when the voltage of VIN pin falls below V_{IN_OVP} falling threshold, the ACOK bit is set to 1, and VIN_OVP bit is cleared.

Cell-Balance

The JW3902 integrates cell-balance for 2 cells application. The chip activates the cell-balance function depending on the voltage V_{BAL} on BAL pin. If V_{BAL} is logic low ($R_{BAL}<100k$), the cell-balance is disabled; if V_{BAL} is logic high ($R_{BAL}>150k$), the cell-balance is enabled, and the chip works on auto balance, host balance or disable balance according to BAL_SEL bits in REG03 register.

Auto Balance

Only when JW3902 enters into charge mode and BAL_SEL=01b, the chip can work on auto balance. The device keeps monitoring each cell voltage. Once it detects that one or two cells voltage are above cell balance start voltage V_{BALST} (decided by BAL_START bit in REG05 register) and the voltage difference V_{DIFF} between two cells is above Balance Threshold ΔV_{CELL} (set by BAL_DIFF bit in REG05 register), it turns on the cell discharging path for the higher voltage cell lasting for 1s. Then if V_{DIFF} detected by the device is below ΔV_{CELL} , the chip turns off the cell discharging path, otherwise it repeats the above discharging and detecting process.

Whichever cell voltage is above charging stop

voltage V_{CHGSTOP} (set by BAL_CHGSTOP bit in REG05) during cell-balance, the chip stops charging. Only when cell-balance is disabled or both the two cells voltages are below V_{CHGSTOP} , the device soft starts up and charges.

Host Balance

when BAL_SEL=10b, the chip can work on host balance. This mode requires MCU to detect each cell voltage, turn on the corresponding cell discharging path for the higher voltage cell by setting BAL_BAT bits in REG03 register.

In host balance mode, whichever cell voltage drops below $V_{\text{BAT_UVP}}$, the chip turns off the corresponding cell discharging path and clears the corresponding BAL_BAT bit which cannot be set to 1 before protection removing, in order to forbid the under-voltage cell's host balance. The other no under-voltage cell's host balance function is unaffected.

Prohibition of Balance

When BAL_SEL=00b, the chip works on prohibition of balance, and invalid writes BAL_BAT bits in REG03 register. If the battery charge voltage is set above 12V, the device clears BAL_SEL bits automatically.

When NTC or TJ_OTP protection occurs, both automatic and host balance are suspended.

Protection

The JW3902 guarantees robustness with comprehensive protection, including input over-voltage protection, battery under-voltage and over voltage protection, charging timeout, battery temperature protection, watchdog timeout and thermal shutdown.

All the protections triggered in charge mode can be resumed automatically, when the faults are

removed.

Input Over-Voltage Protection (VIN_OVP)

When the voltage of VIN pin rises above $V_{\text{IN_OVP}}$ rising threshold, the chip stops switching and sets both VIN_OVP bit in REG07 register and VIN_OVP_INT bit in REG09 register to 1; when the voltage of VIN pin falls below $V_{\text{IN_OVP}}$ falling threshold, VIN_OVP bit is cleared and the device soft starts up to the presetting value; the VIN_OVP_INT bit can be cleared by writing 1 to itself.

Battery Under-Voltage Protection (BAT_UVP)

In host balance mode, whichever cell voltage drops below $V_{\text{BAT_UVP}}$, the chip turns off the corresponding cell discharging path and clears the corresponding BAL_BAT bit which cannot be set to 1 before protection removing, in order to forbid the under-voltage cell's host balance. The other no under-voltage cell's host balance function is unaffected.

Battery Over-Voltage Protection (BAT_OVP)

In 3 cells application or 2 cells application which disable cell balance function (BAL_SEL bits in REG03 register is set to 00b), if the total battery voltage rises above $V_{\text{BAT_OVP}}$ rising threshold, the chip stops switching and sets both BAT_OVP bit in REG07 register and BAT_OVP_INT bit in REG09 register to 1; when the total battery voltage falls below $V_{\text{BAT_OVP}}$ falling threshold, BAT_OVP bit is cleared and the device soft starts up to the presetting value; the BAT_OVP_INT bit can be cleared by writing 1 to itself.

In 2 cells application which enable cell balance function (BAL_SEL \neq 00b), whichever cell voltage rises above charging stop voltage V_{CHGSTOP} (set by BAL_CHGSTOP bit in REG05) during cell-balance, the chip stops switching

and sets both BAT_OVP bit in REG07 register and BAT_OVP_INT bit in REG09 register to 1; when every cell voltage falls below V_{IN_OVP} falling threshold, BAT_OVP bit is cleared and the device soft starts up to the presetting value; the BAT_OVP_INT bit can be cleared by writing 1 to itself.

NTC Protection (NTC_FAULT)

For battery protection during charge mode, the device monitors the battery temperature through NTC pin. When the voltage of the NTC pin is outside the thresholds, the charge progress is suspended. In addition, STAT pin blinks at 1Hz to inform fault condition. Once temperature returns within thresholds, the charge is recovered.

A 10k 103-AT thermistor is needed to be connected between NTC pin and GND for NTC protection. The thresholds of NTC protection can be set by NTCH_SEL bits and NTCL_SEL bits in REG03 register.

When the NTC resistor voltage is outside of the setting temperature thresholds, the chip stops switching and sets NTC_FAULT bit in REG07 register to 1. If the chip is in charge mode, it can resume switching and clear the NTC_FAULT bit, when the NTC voltage is within the thresholds again.

Charging Timeout (CHG_FAULT)

When working in charge mode, the JW3902 uses an internal timer to terminate the charging process, once the time it stays in charge mode exceeds the value set by CHG_TIMER bits in REG01 register.

Once the chip enters into charge mode, the timer starts working. When the timer is expired, the chip stops switching and sets CHG_FAULT bit in REG07 register to 1.

When the charge timer is expired, it can be reset by writing 1 to TIMER_RST bit in REG05 register. Once the charge timer is reset, the CHG_FAULT bit is cleared automatically and the chip resumes switching and soft starts up.

When the chip exits charge mode (EN_CHG bit=0b or EN pin=logic low or ICHG bits=0) or enters into IDLE/shutdown mode from charge mode, the timer stops and is reset automatically, and the CHG_TIMEOUT bit is cleared as well. When the CHG_STAT bits in REG06 is set to 11b, the timer also stops and is reset automatically.

There are two following points should be noted. Firstly, if the device stops charging because of protection, the timer is reset automatically and continues timing. Secondly, the timer can be reset by setting TIMER_RST=1, but it doesn't stop counting.

Watchdog Timer (WD_FAULT)

The JW3902 offers a watchdog timer to ensure the reliability of I2C communication. Once the watchdog timer is expired(20s), the chip stops switching, resets related registers and sets WD_FAULT bit in REG07 register to 1. The fault can be removed by a writing 1 command to WD_RES bit in REG05 register, then the chip resumes switching and soft starts up. Whenever writing 1 to WD_RES bit, the watchdog timer can be reset.

The watchdog timer only works in charge mode. When the chip enters into IDLE mode, the timer stops and is reset.

Thermal Shutdown (TJ_OTP)

When the junction temperature continues rising above T_{SHUT} , the device enters into thermal shutdown mode, in which it stops switching and sets both TJ_OTP bit in REG07 register and

TJ_OTP_INT bit in REG08 register to 1. If the device is in charge mode, it can resume switching clear TJ_OTP bit, when the junction temperature drops below $T_{SHUT}-20^{\circ}C$. TJ_OTP_INT bit is cleared by writing command 1 to itself.

When the chip enters into IDLE mode, the fault is removed automatically, and TJ_OTP bit is cleared as well.

I2C Interface

The JW3902 integrates an I2C interface to provide flexible solutions for different applications. The JW3902 always works as a salve module with a 7-bit address 0x6B (110_1011xb). The integrated I2C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

To ensure the reliability of the communication, after the chip is powered up or EN pin is toggled from low to high, the host must wait for at least 1ms before sending any I²C command.

Start and Stop Conditions

A HIGH to LOW transition on SDA line while SCL is HIGH defines a START condition, and a LOW to HIGH transition on SDA line while SCL is HIGH defines a STOP condition.

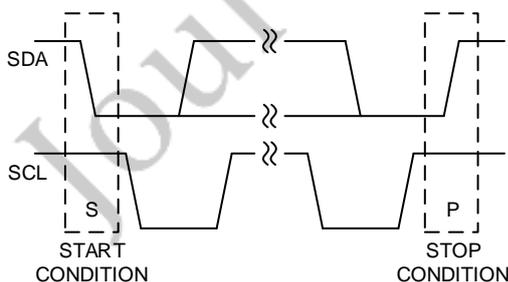


Figure 3. START and STOP conditions

The START and STOP conditions can only be sent by the master.

Data Validity

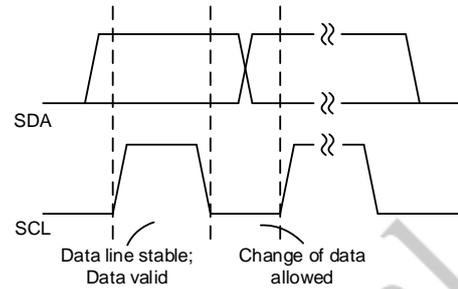


Figure 4. Data validity

The data on SDA line must be stable during the HIGH period of the SCL, unless a START or STOP condition generated. The HIGH or LOW state of SDA line can only change when the clock signal on SCL line is LOW.

Byte Format

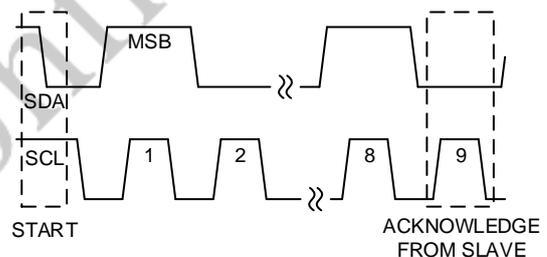


Figure 5. Data transfer on the I2C bus

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte until it has performed some other function, it can hold the clock line SCL LOW to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after each byte.

The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte can be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

Single Read and Write

The device supports single read and write.

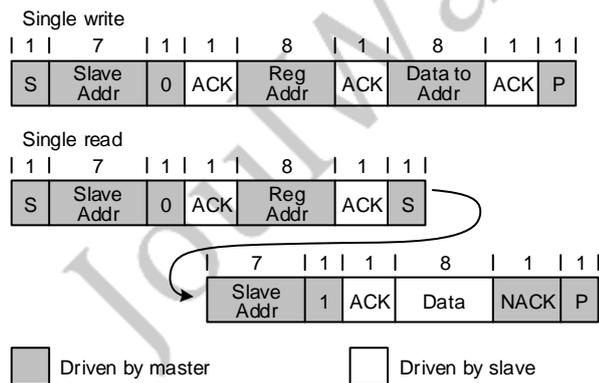


Figure 6. Single read and single write

Multi-Read and Multi-Write

The device supports multi-read and multi-write.

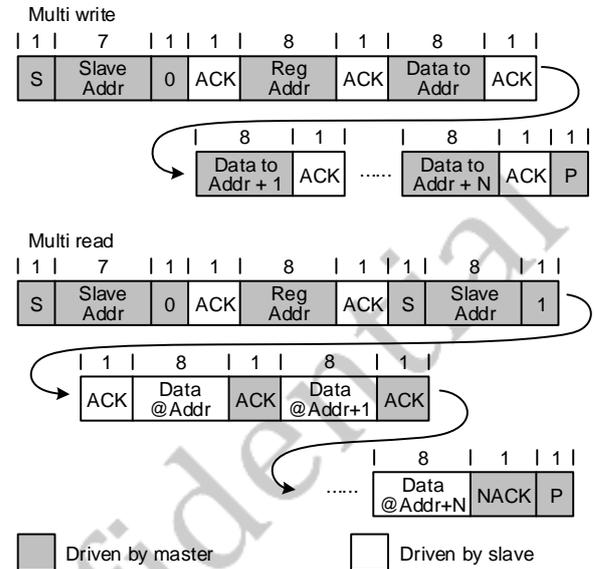


Figure 7. Multi read and multi write

Interrupt

When any bit in REG08 register changes from 0 to 1. The chip sends an active low, 0.512ms pulse at INT pin to inform the host, as shown in the figure below.

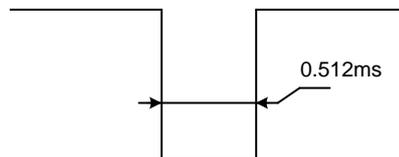


Figure 8. Interrupt pulse at INT pin

User can disable the interrupt output of any bit by setting its corresponding bit in REG09 register to 0. When the enable bit is cleared, the corresponding status bit is still set, but the chip does not send an interrupt pulse at INT pin.

REGISTER MAP

Register	Address	Reset Value
REG00	0x00	0x2C
REG01	0x01	0xD8
REG02	0x02	0x89
REG03	0x03	0x51
REG04	0x04	0x64
REG05	0x05	0x00
REG06	0x06	0x00
REG07	0x07	0x00
REG08	0x08	0x00
REG09	0x09	0xFF

REG00

BIT	NAME	POR	Type	Reset	Description	Comment
7	BATCV [2]	0	W/R	By POR By REG_RST By Watchdog	000 – 8.15V	Battery voltage regulation target selector Default 8.4V, BATCV=001 VIN_PRESENT=0 Clear it to default value
6	BATCV [1]	0	W/R		001 – 8.4V	
5	BATCV [0]	1	W/R		010 – 8.5V	
					011 – 8.7V	
					100 – 12.23V	
					101 – 12.6V	
110 – 12.75V						
111 – 13.05V						
4	VINDPM [2]	0	W/R	By POR By REG_RST By Watchdog	400mV	Input voltage limit threshold selector Offset: 4.1V Default value 4.4V VIN_PRESENT=0 Clear it to default value
3	VINDPM [1]	1	W/R		200mV	
2	VINDPM [0]	1	W/R		100mV	
1	Reserved	0	R	NA		
0	Reserved	0	R	NA		

REG01

BIT	NAME	POR	Type	Reset	Description	Comment
7	CHG_TIMER [1]	1	W/R	By POR	00 – Disable charge timer	Charge time-out timer
6	CHG_TIMER [1]	1	W/R	By REG_RST	timer Default	Default: 24hrs

				By Watchdog	01 – 6 hrs 10 – 12 hrs 11 – 24 hrs	VIN_PRESENT=0 Clear it to default value
5	ICHG [5]	0	W/R	By POR By REG_RST By Watchdog	1600mA	Programmable charge current selector Offset: 0mA Range: 0~3.15A; Default value: 1200mA, ICHG=0x18; LSB = 50mA VIN_PRESENT=0 Clear it to default value ICHG=0, stop charging
4	ICHG [4]	1	W/R		800mA	
3	ICHG [3]	1	W/R		400mA	
2	ICHG [2]	0	W/R		200mA	
1	ICHG [1]	0	W/R		100mA	
0	ICHG [0]	0	W/R		50mA	

REG02

BIT	NAME	POR	Type	Reset	Description	Comment			
7	FSW [1]	1	W/R	By POR By REG_RST	00 – 500KHz 01 – 750KHz 10 – 1MHz 11 – 1.5MHz	System switching frequency selector Default: 1MHz VIN_PRESENT=0 Clear it to default value			
6	FSW [0]	0	W/R						
5	ITERM [2]	0	R/W				By POR	200mA	Termination Current selector Offset: 50mA Default: 100mA VIN_PRESENT=0 Clear it to default value
4	ITERM [1]	0	R/W				By REG_RST	100mA	
3	ITERM [0]	1	R/W	By Watchdog	50mA				
2	IPRECHG [2]	0	R/W	By POR	200mA	Pre-charge Current selector Offset: 50mA Default: 100mA VIN_PRESENT=0 Clear it to default value			
1	IPRECHG [1]	0	R/W	By REG_RST	100mA				
0	IPRECHG [0]	1	R/W	By Watchdog	50mA				

REG03

BIT	NAME	POR	Type	Reset	Description	Comment	
7	NTCH_SEL [1]	0	W/R	By POR By REG_RST By Watchdog	00 – disable 01 – 45°C 10 – 55°C 11 – 60°C	NTC over temperature threshold selector Default: 45°C VIN_PRESENT=0 Clear it to default value	
6	NTCH_SEL [0]	1	W/R				
5	NTCL_SEL [1]	0	W/R				00 – disable

4	NTCL_SEL [0]	1	W/R		01 – 0°C 10 – -5°C 11 – -10°C	selector Default: 0°C VIN_PRESENT=0 Clear it to default value
3	BAL_BAT1	0	W/R		0 – turn off BAT1 Balance 1 – turn on BAT1 Balance	Default: turn off BAT1 Balance Cell 1 undervoltage, the bit cleared automatically; BAL_SEL=00b, the bit cleared automatically
2	BAL_BAT0	0	W/R		0 – turn off BAT0 Balance 1 – turn on BAT0 Balance	Default: turn off BAT0 Balance Cell 0 undervoltage, the bit cleared automatically; BAL_SEL=00b, the bit cleared automatically
1	BAL_SEL [1]	0	W/R		00– Disable Balance	Default: Auto Balance Decoder logic low or battery charge voltage above 12V clear the bit automatically
0	BAL_SEL [0]	1	W/R		01 – Auto Balance 10 – Host control Balance 11 – Reserved	

REG04

BIT	NAME	POR	Type	Reset	Description	Comment
7	Reserved	0	R	NA		
6	EN_CHG	1	R/W	By POR By REG_RST By Watchdog	0 – Charge Disable 1 – Charge Enable	Default: Charge Enable VIN_PRESENT=0 Clear it to default value
5	EN_TERM	1	W/R		0 – Disable full-charge detect 1 – Enable full-charge detect	Full charge enable bits Default: Enable VIN_PRESENT=0 Clear it to default value
4	EN_WD	0	W/R	By POR By REG_RST	0 – Disable watchdog timer 1 – Enable watchdog timer	Watchdog timer enable bit Default: Disable
3	EN_TMR2X	0	R/W	By POR	0 – Disable	Default: Disable

				By REG_RST By Watchdog	1 – Safety timer slowed by 2X during input VINDPM or thermal regulation	VIN_PRESENT=0 Clear it to default value
2	TREG_SEL	1	W/R		0 – 130°C 1 – 145°C	Charge temperature loop threshold selector Default: 145°C VIN_PRESENT=0 Clear it to default value
1	Reserved	0	R	NA		
0	Reserved	0	R	NA		

REG05

BIT	NAME	POR	Type	Reset	Description	Comment
7	BAL_DIFF	0	W/R	By POR By REG_RST By Watchdog	0 – 30mV 1 – 40mV	Balance voltage difference threshold selector Default: 30mV
6	BAL_CHGSTOP [1]	0	W/R	By POR By REG_RST	00 – 4.1V 01 – 4.05V	Charging stops voltage threshold during battery balance Default: 4.1V
5	BAL_CHGSTOP [0]	0	W/R	By Watchdog	10 – 4.0V 11 – 3.7V	
4	BAL_START	0	W/R	By POR By REG_RST By Watchdog	0 – 3.7V 1 – 4.05V	Automatic balance starts voltage threshold during charging Default: 3.7V
3	Reserved	0	R	NA		
2	TIMER_RST	0	W/R	By POR		Write command 1 to reset charge timeout timer and clear CHG_FAULT bit
1	WD_RST	0	W/R	By POR		Write command 1 to reset watchdog timer and clear WD_FAULT bit
0	REG_RST	0	W/R	By POR		Write command 1 to reset all register

REG06

BIT	NAME	POR	Type	Reset	Description	Comment
7	CHG_STAT[1]	0	R	NA	00 – Not charge	Charge status description bits
6	CHG_STAT[0]	0	R		01 – Trickle charge phase 10 – CC charge phase 11 – Charge termination	
5	VINDPM_STAT	0	R	NA	0 – VIN not DPM 1 - VINDPM	Input voltage limit flag
4	THERMAL_STAT	0	R	NA	0 – Not thermal regulate 1 – Thermal regulate	Temperature loop flag bit
3	ACOK	0	R	By POR	0 – adapter not OK 1 – adapter OK	VIN_PRESENT=1&VIN<VIN_OVP for 30ms
2	VIN_PRESENT	0	R		0 – VIN is not present 1 – VIN is present	VIN>VIN_UVLO for 256ms
1	Reserved	0	R			
0	Reserved	0	R			

REG07

BIT	NAME	POR	Type	Reset	Description	Comment
7	VIN_OVP	0	R	By POR	0 – VIN not over voltage 1 – VIN over voltage	VIN over-voltage protection flag bit 1. Fault removed clears the bit automatically;
6	TJ_OTP	0	R		0 – Junction temperature OK 1 – Junction over temperature	Chip over-temperature protection flag bit 1. Fault removed clears the bit automatically;
5	NTC_FAULT	0	R		0 – NTC thermistor	Battery temperature-protection

					voltage OK 1 – NTC thermistor voltage over range	flag bit 1. Fault removed clears the bit automatically; 2. Forbidding NTC clears the bit automatically;
4	BAT_OVP	0	R		0 – BAT not over voltage 1 – BAT over voltage	Battery over-voltage protection flag bit 1. Fault removed clears the bit automatically;
3	CHG_FAULT	0	R		0 – Charge timer OK 1 – Charge timeout	Charge timeout fault flag bit 1. Writing 1 to TIMER_RST Clears it to 0; 2. Forbidding charge timeout timer clears it to 0; 3. EN=0 or EN_CHG=0 or IDLE mode clears it to 0;
2	WD_FAULT	0	R		0 – Normal Default 1 - Watchdog timer expiration	Watchdog overflow fault flag bit 1. Writing 1 to WD_RST Clears it to 0; 2. Forbidding watchdog timer clears it to 0;
1	Reserved	0	R			
0	Reserved	0	R			

REG08

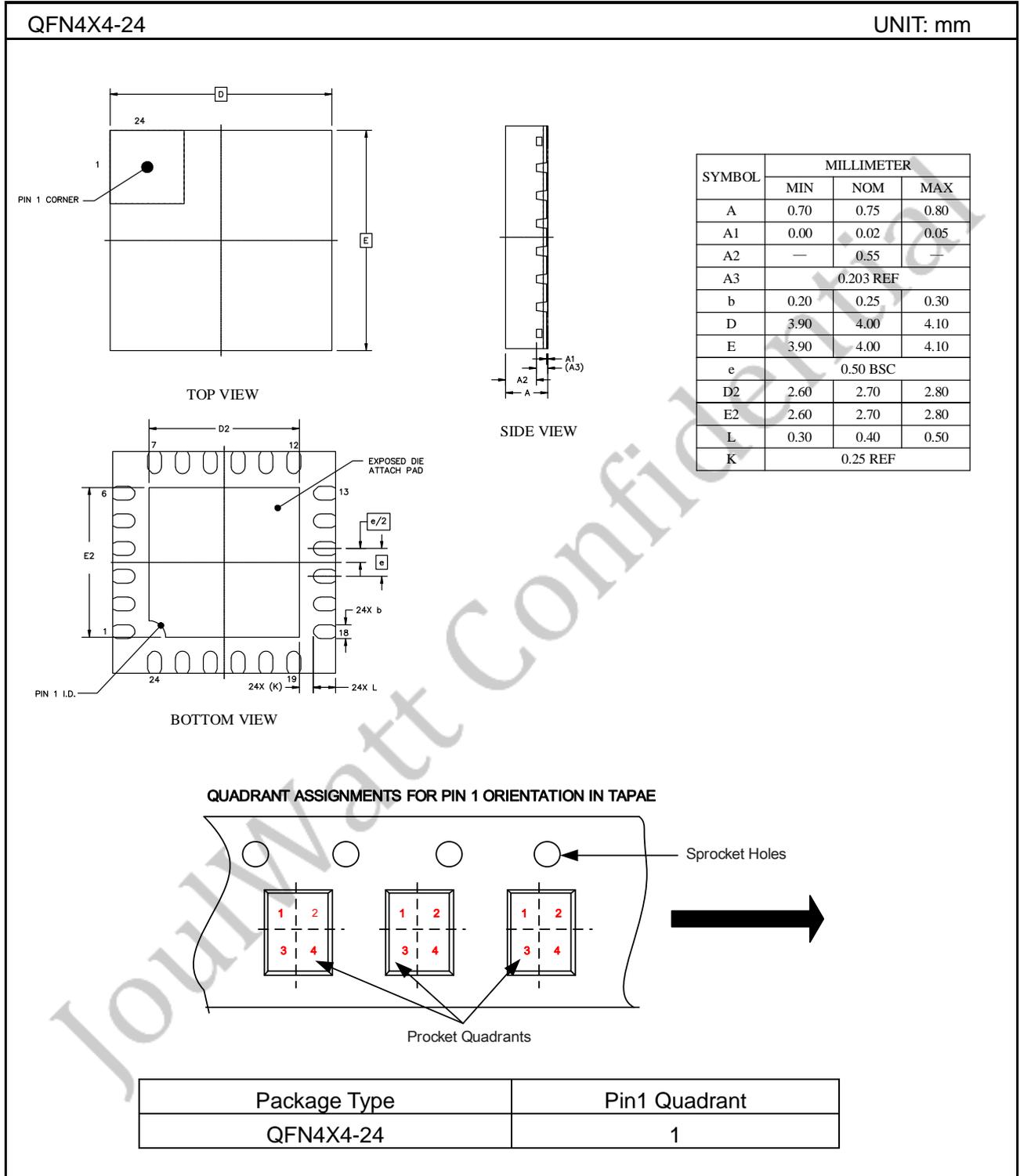
BIT	NAME	POR	Type	Reset	Description	Comment
7	VIN_OVP_INT	0	W/R	By POR By REG_RST	0 – VIN not over voltage 1 – VIN over voltage	VIN over-voltage protection interrupt request flag bit Writing 1 to VIN_OVP_INT Clears it to 0
6	TJ_OTP_INT	0	W/R		0 – Junction temperature OK 1 – Junction over temperature	Chip over-temperature protection interrupt request flag bit Writing 1 to TJ_OTP Clears it to 0
5	NTC_FAULT_INT	0	W/R		0 – NTC thermistor voltage OK	Battery temperature-protection interrupt request flag bit

					1 – NTC thermistor voltage over range	Writing 1 to NTC_FAULT Clears it to 0
4	BAT_OVP_INT	0	W/R		0 – BAT not over voltage 1 – BAT over voltage	Battery over-voltage protection interrupt request flag bit Writing 1 to BAT_OVP_INT Clears it to 0
3	VIN_INT	0	W/R		0 – no VIN plug or unplug event 1-VIN plug or unplug event	Adapter plug event interrupt request flag bit Writing 1 to VIN_INT Clears it to 0
2	CHG_INT	0	W/R		0 – no full charge or recharge event 1-occurs full charge or recharge event	Battery full charge and recovery interrupt request flag bit Writing 1 to CHG_INT Clears it to 0
1	Reserved	0	R			
0	Reserved	0	R			

REG09

BIT	NAME	POR	Type	Reset	Description	Comment
7	VIN_OVP_EN	1	W/R	By POR By REG_RST	0 – disable 1 – enable	VIN over-voltage protection interrupt enable bit
6	TJ_OTP_EN	1	W/R		0 – disable 1 – enable	Chip over-temperature protection interrupt enable bit
5	NTC_FAULT	1	W/R		0 – disable 1 – enable	Battery temperature-protection interrupt enable bit
4	BAT_OVP_EN	1	W/R		0 – disable 1 – enable	Battery over-voltage protection interrupt enable bit
3	VIN_INT_EN	1	W/R		0 – disable 1 – enable	Adapter plug event interrupt enable bit
2	CHG_INT_EN	1	W/R		0 – disable 1 – enable	Battery full charge and recovery interrupt enable bit
1	CHG_FAULT_EN	1	W/R		0 – disable 1 – enable	Charge timeout fault interrupt enable bit
0	WD_FAULT_EN	1	W/R		0 – disable 1 – enable	Watchdog overflow fault interrupt enable bit

PACKAGE OUTLINE



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