JWH5276

7V/6A

Sync. Step-Down Converter

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JWH®5276 is a monolithic buck switching regulator based on a proprietary I2 control for fast transient response. Operating with an input range of 2.95V~7V, JWH5276 delivers 6A of continuous output current with integrated two MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external schottky diode.

JWH5276 guarantees robustness with output short protection, thermal protection, current run-away protection, and input under voltage lockout.

JWH5276 is available in QFN3X3-16 packages, which provide a compact solution with minimal external components.

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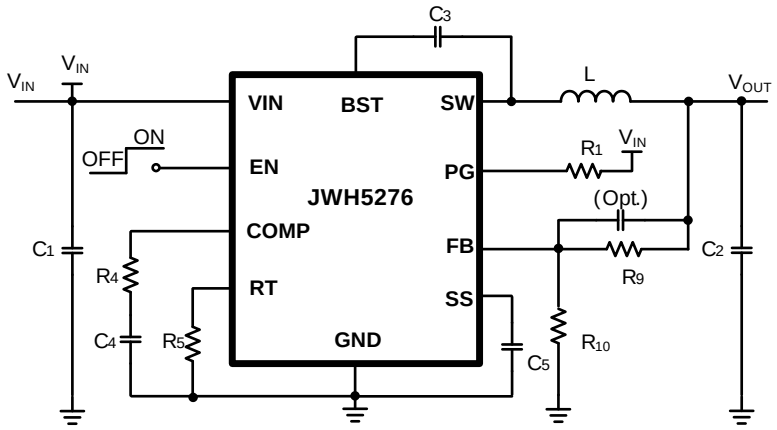
FEATURES

- 2.95V to 7V operating input range
- Up to 6A output current
- Internal 12mΩ High-Side and 12mΩ Low-Side MOSFETs
- Adjustable switching frequency
- Adjustable soft-start time
- Power good indicator
- Input under voltage lockout
- Output short circuit protection
- Thermal protection
- Available in QFN3X3-16 package

APPLICATIONS

- Low-voltage, High Density Power System
- POL Regulation for High-performance DSPs, FPGAs, ASICs and Microprocessors
- Gaming, DTV and Set-top Boxes
- Hard Disk Drives

TYPICAL APPLICATION



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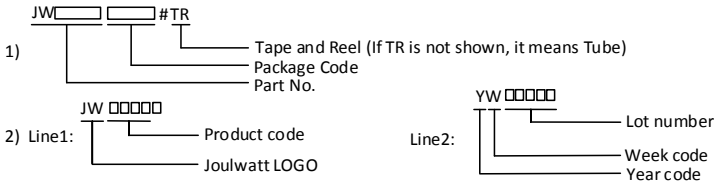
ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JWH5276QFNA#TR	QFN3X3-16	JWH5276 YW□□□□□	Green

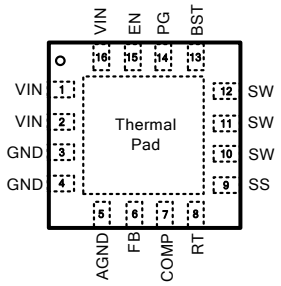
Notes:



3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION

TOP VIEW



ABSOLUTE MAXIMUM RATING[1)]

Input Supply Voltage (V_{IN}).....-0.3V to 8V
EN Voltage (V_{EN}) .....-0.3V to 8V
PG Voltage (V_{PG}).....-0.3V to 8V
SW Voltage (V_{SW}).....-0.3V(-2V for 20ns; -4V for 5ns) to 8V(10V for 20ns; 12V for 5ns)
BST Voltage (V_{BST}).....V_{SW} +4V
FB, COMP, SS, RT Pins.....-0.3V to 4V
Operating Junction Temp. [2)] .....-40 ºC ~150ºC
Storage Junction Temp. [2)] ..... -65 ºC ~150ºC
Lead Temperature 260ºC

ESD RATINGS

Human body model (HBM), per ANSI/ESDA/JEDEC JS-001..... ±2000V
Charged device model (CDM), per JEDEC specification JESD22- V C101..... ±500V

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RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage V_{IN}..... 2.95V to 7V
Output Voltage V_{OUT}.....0.6V to VIN*Dmax

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
QFN3X3-16	44	4.1ºC/W

Notes:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWH5276 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

4) Measured on JESD51-7, 4-layer PCB

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ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_J=-40℃~150℃，Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{IN} Under Voltage Lock-out Rising Threshold	V_{IN_R}	V_{IN} rising	2.6	2.77	2.9	V
V_{IN} Under Voltage Lock-out Falling Threshold	V_{IN_F}	V_{IN} falling	2.31	2.48	2.61	V
Shutdown Supply Current	I_{SD}	V_{EN}=0V, T_A= 25℃		1.7	3	μA
Supply Current	I_Q	V_{EN}=2V, V_{FB}=1V, Non-switching		300	500	μA
Feedback Voltage	V_{FB}	2.95V≤V_{IN}≤7V	594	600	606	mV
Top Switch Resistance	$R_{DS(ON)T}$	I_{SW} = 500mA		12	20	mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$	I_{SW} = 500mA		12	20	mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=7V, V_{EN}=0V, V_{SW}=0V, T_J=25℃		0.1		μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=7V, V_{EN}=0V, V_{SW}=7V, T_J=25℃		0.1		μA
Error Amplifier Transconductance	g_m	V_{COMP}=1V		260		uA/V
Error Amplifier Source and Sink		V_{COMP}=1V, 100mV overdrive		±22		uA
COMP to I_{switch} gain				14		A/V
Top Switch Current Limit	I_{LIM_TOP}		9.5	10.5	12.5	A
Bottom Switch Current Limit	I_{LIM_BOT}		6	7.5	9.5	A
Bottom Switch Negative Current Limit	$I_{LIM\_BOT\_NEG}$			-4.5		A
Cycles Before Entering Hiccup During OC[5)]				4150		cycle
Hiccup Off Time[5)]			12	16	20	ms
EN Rising Threshold Voltage	V_{EN_H}		1.25	1.3	1.35	V
EN Falling Threshold Voltage	V_{EN_L}		1.13	1.18	1.23	V
EN Input Current	I_{EN_H}	V_{EN_H} +50mV		-3.5		μA
	I_{EN_L}	V_{EN_L} -50mV		-0.55		μA
EN Turn On Delay[5)]	T_{ON_Delay}	From EN high to switching, T_J=+25℃		70	200	μs
Power Good Output Low	V_{PG_OL}	I_{PG}=-2.5mA			0.3	V
Power Good Lower Threshold Voltage	$V_{PG\_TH\_L}$	FB rising	90%	93.5%	97%	V_{REF}
		FB falling	88%	91.5%	95%	V_{REF}
Power Good Upper Threshold Voltage	$V_{PG\_TH\_H}$	FB rising	113%	116.5%	120%	V_{REF}
		FB falling	111%	114.5%	118%	V_{REF}

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V_{IN}=5V, T_J=-40℃~150℃，Unless otherwise stated.						
Item	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Power Good Delay Time	t_{PG_DLY1}	PG from low to high	10	15	20	μs
	t_{PG_DLY2}	PG from high to low	8	13	18	μs
Soft-Start Charge Current	I_{SS_CHAR}	V_{SS} > 0.1V	1.5	2	2.5	μA
		V_{SS} < 0.1V	30	39	50	μA
Soft-Start Discharge Current	$I_{SS\_DIS\ CHAR}$	V_{SS}= 4V	1	2.8		mA
Switching Frequency Range	F_{SW}	I_{OUT} = 1A	400		2000	kHz
Switching Frequency	F_{SW}	R_T = 39.2 kΩ	850	1000	1150	kHz
RT Voltage		R_T = 39.2 kΩ		0.5		V
Minimum On-Time[5)]	t_{ON_MIN}			110	130	ns
Minimum Off-Time	t_{OFF_MIN}			80	110	ns
Thermal Shutdown[5)]	T_{TSD}			170		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYST}			20		°C

Note：

5) Guaranteed by design.

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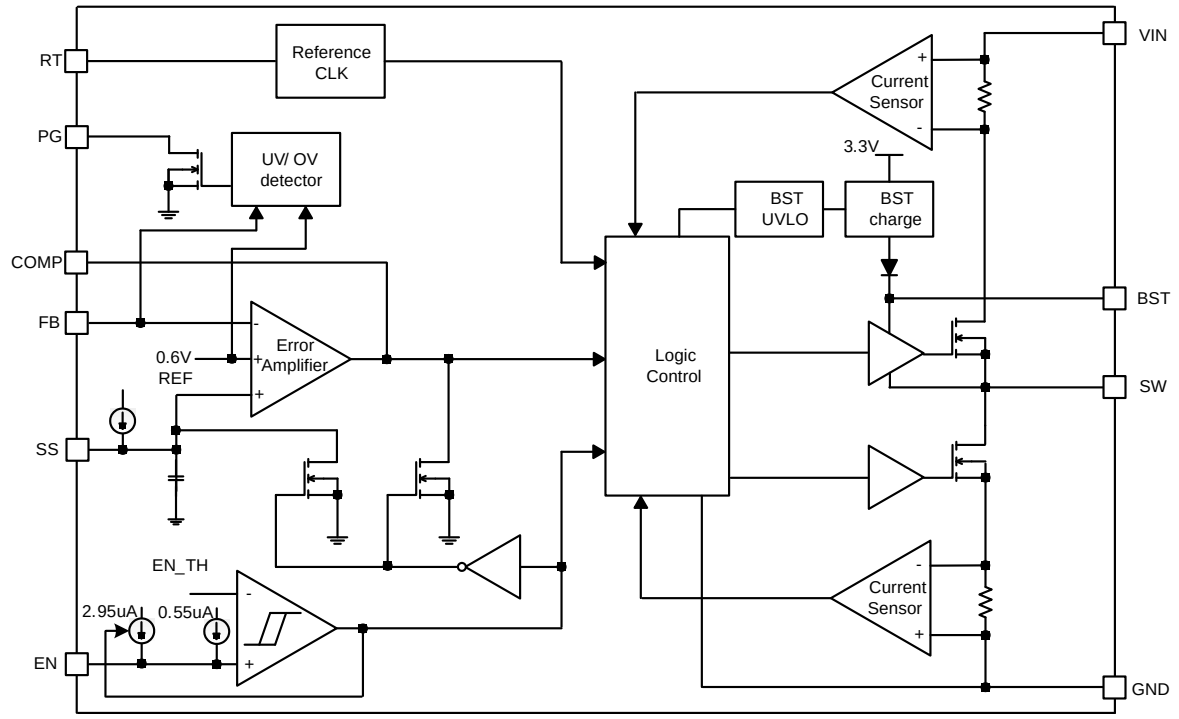
PIN DESCRIPTION

Pin	Name	Description
1, 2, 16	VIN	Supply voltage for power stage. Connect a 2.95V to 7V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3, 4	GND	Ground pin.
5	AGND	Analog ground should be tied to GND close to the device.
6	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6 V. Connect a resistive divider at FB.
7	COMP	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
8	RT	Switching frequency setting pin.
9	SS	Soft-start time setting pin
10, 11, 12	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
13	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
14	PG	Output power good indicator (High=V_{OUT} ready, Low=V_{OUT} below nominal regulation); open drain (requires pull-up resistor).
15	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator. Float to enable.
	Exposed Pad	GND pin must be connected to the exposed power pad for proper operation. This power pad should be connected to any internal PCB ground plane using multiple vias.

BLOCK DIAGRAM



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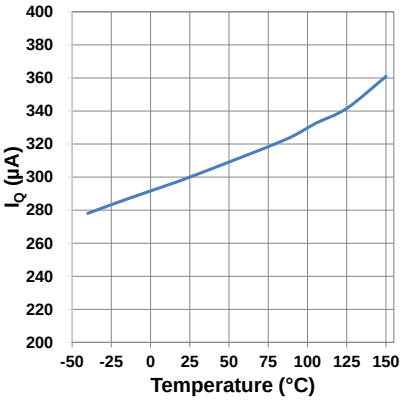
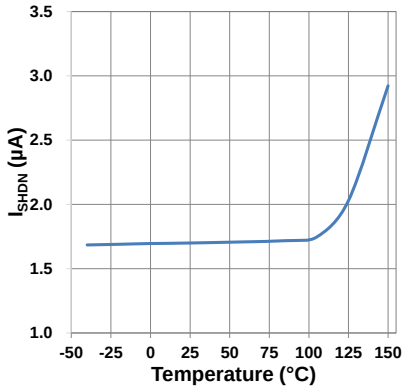
TYPICAL CHARACTERISTICS

VIN =5V, T_J = -40°C to +150°C, unless otherwise noted

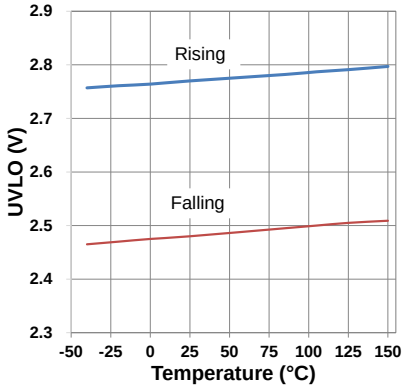
Quiescent Current vs. Temperature



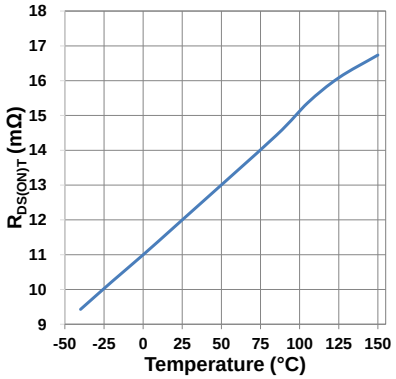
Shutdown Current vs. Temperature



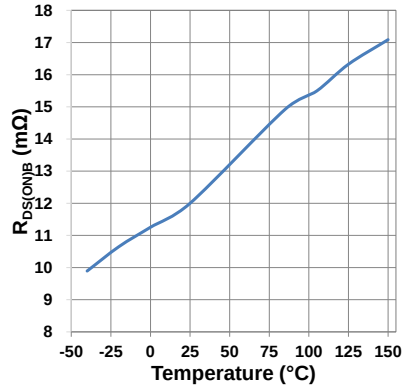
V_{IN} UVLO Threshold vs. Temperature



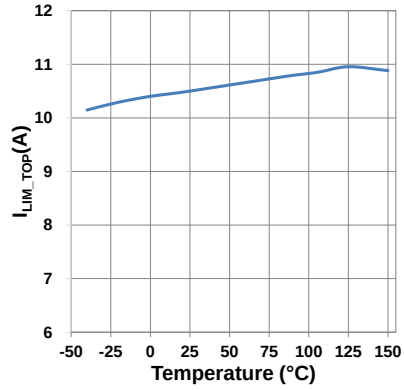
Top Switch Resistance vs. Temperature



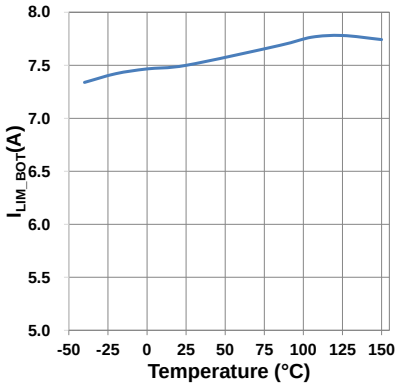
Bottom Switch Resistance vs. Temperature



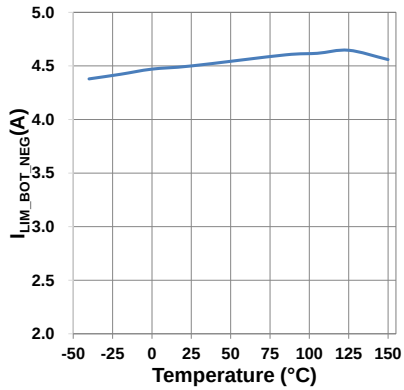
Top Switch Current Limit vs. Temperature



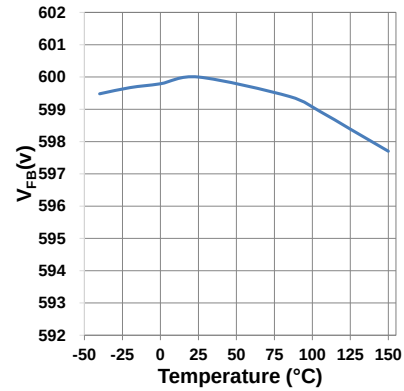
Bottom Switch Current Limit vs. Temperature



Negative Current Limit vs. Temperature



Feedback Voltage vs. Temperature



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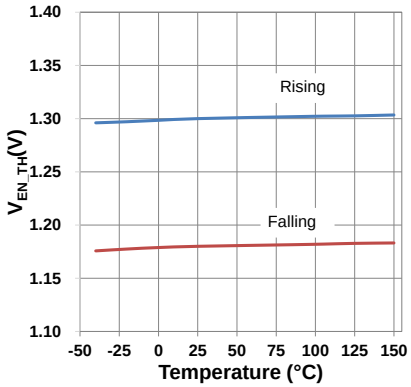
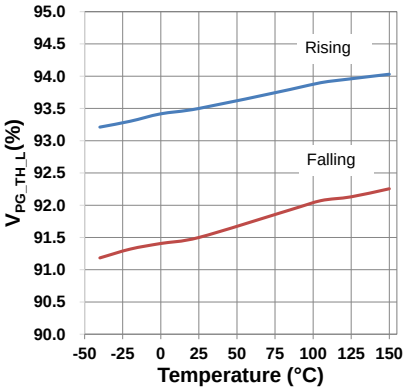
TYPICAL CHARACTERISTICS *(Continued)*

VIN =5V, T_J = -40°C to +150°C, unless otherwise noted

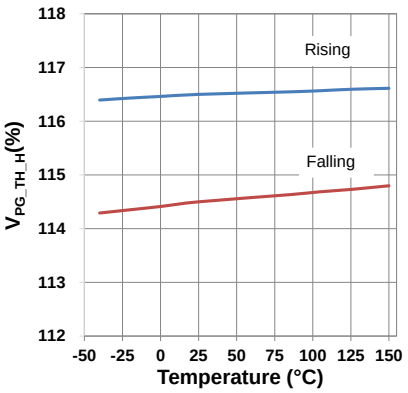
EN Threshold vs. Temperature



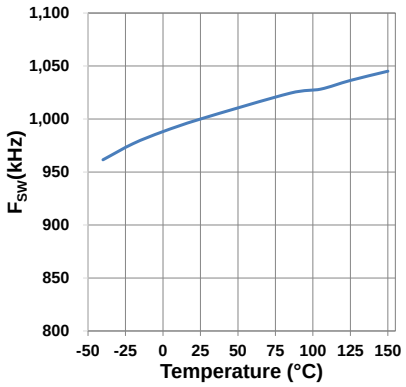
PG Lower Threshold vs. Temperature



PG Upper Threshold vs. Temperature



Frequency vs. Temperature



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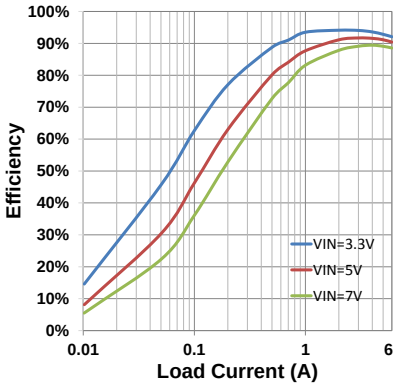
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.33μH, C_{OUT} = 104μF, T_A = +25°C, unless otherwise noted.

Efficiency vs. Load Current

V_{OUT}=1.8V, F_{SW}=1MHz, L=0.33μH



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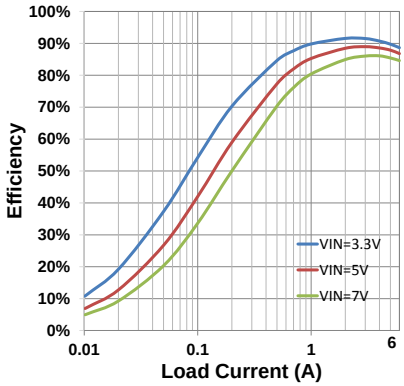
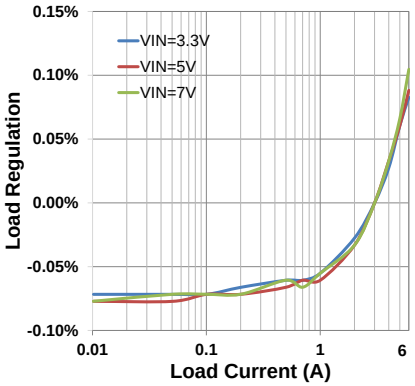


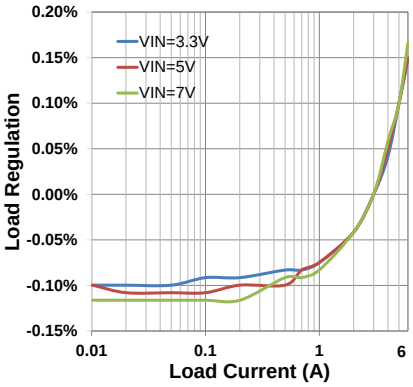
Load Regulation

V_{OUT}=1.8V, F_{SW}=1MHz, L=0.33μH



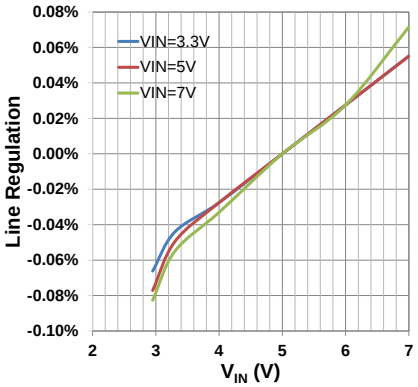
Load Regulation

V_{OUT}=1.2V, F_{SW}=1MHz, L=0.33μH



Line Regulation

V_{OUT}=1.8V, F_{SW}=1MHz, L=0.33μH



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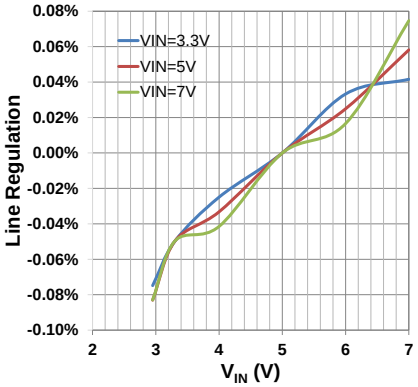
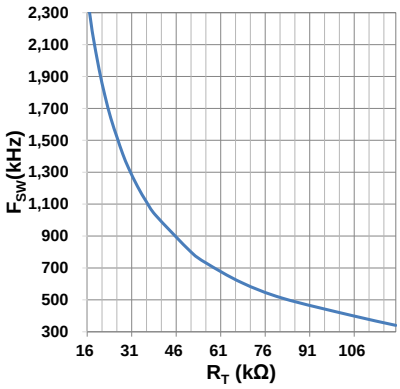
V_{OUT}=1.2V, F_{SW}=1MHz, L=0.33μH



Frequency vs. RT Resistance

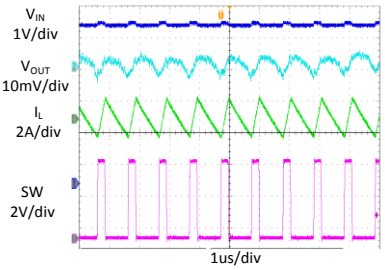


TYPICAL PERFORMANCE CHARACTERISTICS *(Continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.33μH, C_{OUT} = 104μF, T_A = +25°C, unless otherwise noted.

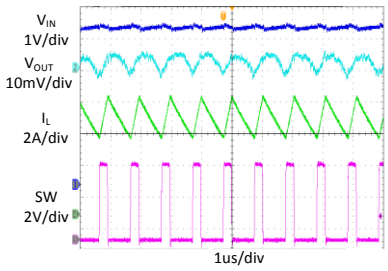
Steady State

I_{OUT}=0A



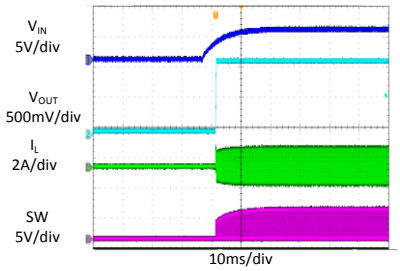
Steady State

I_{OUT}=6A



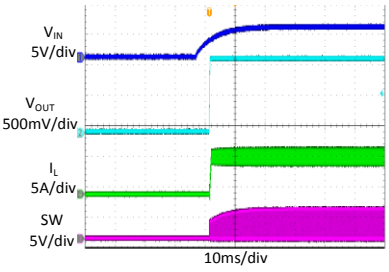
Start-Up through VIN

I_{OUT}=0A



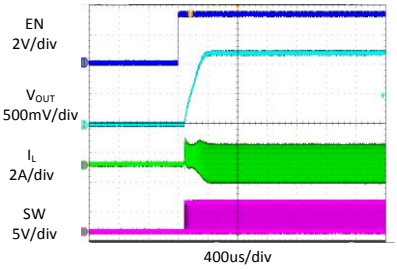
Start-Up through VIN

I_{OUT}=6A



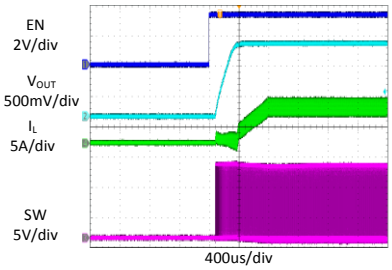
Start-Up through Enable

I_{OUT}=0A



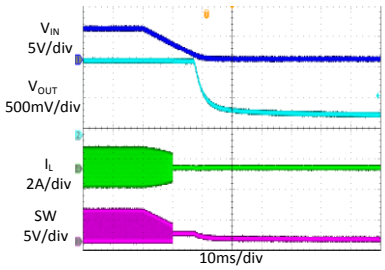
Start-Up through Enable

I_{OUT}=6A



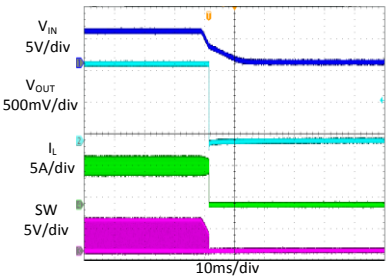
Shutdown through VIN

I_{OUT}=0A



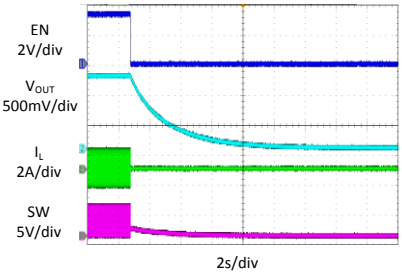
Shutdown through VIN

I_{OUT}=6A



Shutdown through Enable

I_{OUT}=0A



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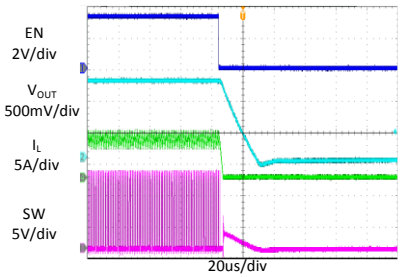
TYPICAL PERFORMANCE CHARACTERISTICS *(Continued)*

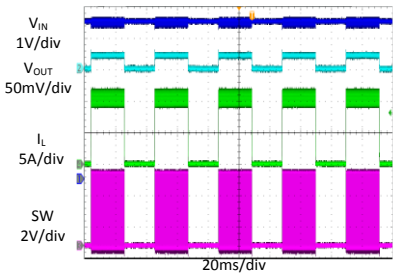
VIN = 5V, Vout = 1.2V, L = 0.33µH, Cout = 104µF, T_A = +25°C, unless otherwise noted.

Shutdown through Enable

I_{OUT}=6A

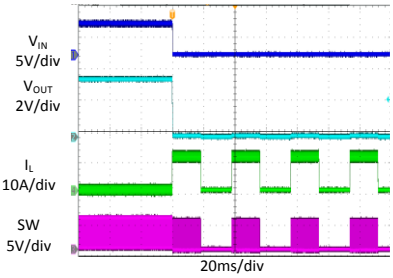


SCP Steady State



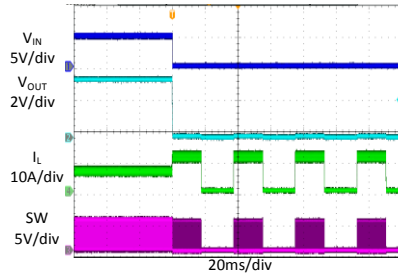
SCP Entry

I_{OUT}=0A



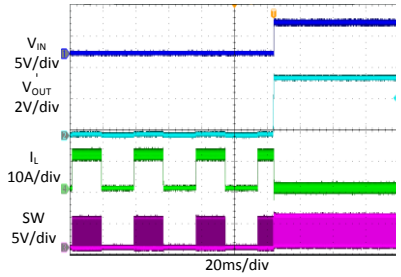
SCP Entry

I_{OUT}=6A



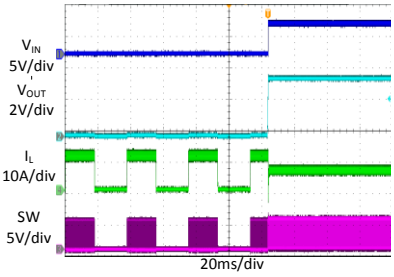
SCP Recovery

I_{OUT}=0A



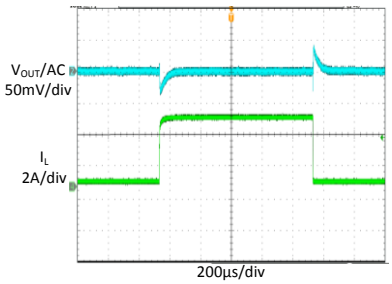
SCP Recovery

I_{OUT}=6A



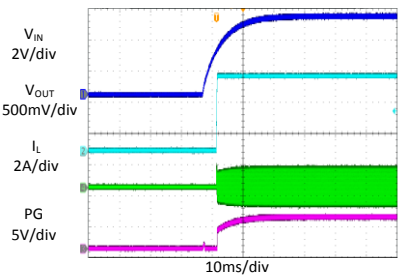
Load Transient

I_{OUT}=0.4A<->4.5A, 1A/µs



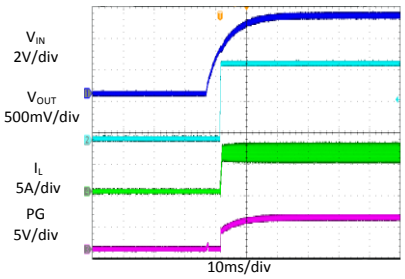
PG in Start-Up through VIN

I_{OUT}=0A



PG in Start-Up through VIN

I_{OUT}=6A



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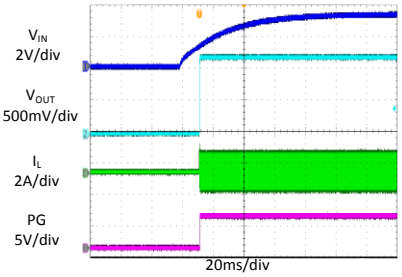
TYPICAL PERFORMANCE CHARACTERISTICS *(Continued)*

VIN = 5V, Vout = 1.2V, L = 0.33μH, Cout = 104μF, T_A = +25°C, unless otherwise noted.

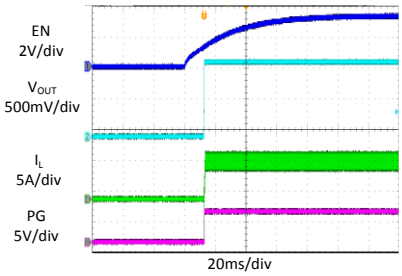
PG in Start-Up through Enable

I_{OUT}=0A



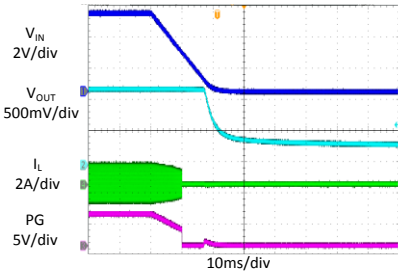
PG in Start-Up through Enable

I_{OUT}=6A



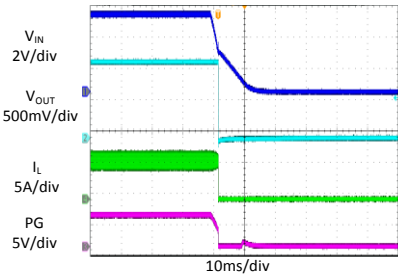
PG in Shutdown through VIN

I_{OUT}=0A



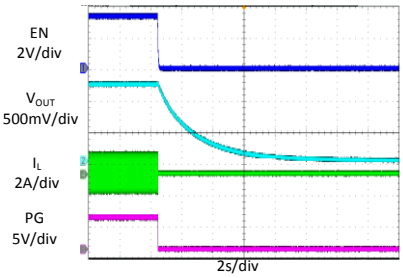
PG in Shutdown through VIN

I_{OUT}=6A



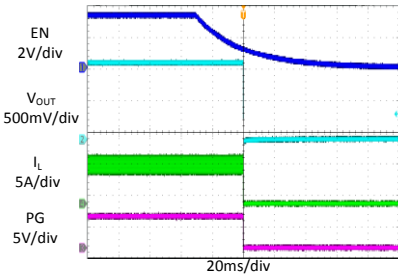
PG in Shutdown through Enable

I_{OUT}=0A

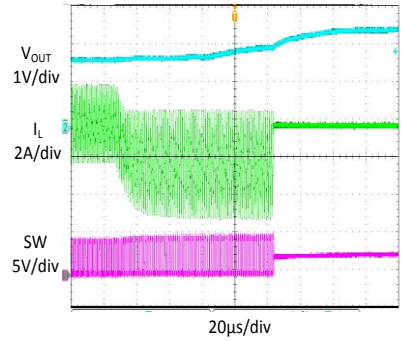


PG in Shutdown through Enable

I_{OUT}=6A



OVP



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FUNCTIONAL DESCRIPTION

The JWH5276 is a synchronous step-down regulator based on a proprietary I2 control for fast transient response. It regulates input voltages from 2.95V~7V down to an output voltage as low as 0.6V, and is capable of supplying up to 6A of load current.

Forced Continuous Current Mode

The JWH5276 utilizes a settable fixed frequency, I2 control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier which drives the COMP pin. Output of the internal error amplifier is compared to the bottom switch current measured internally. When the bottom switch current drops below the COMP voltage level, the bottom switch is turned off and the top switch is allowed to turn on. A proper current ripple determined by the frequency set by RT pin is generated by the current ripple generator, and the sum of the current ripple and the error amplifier output is used as the top current reference. When the top current reaches this current reference, the top switch is turned off and the bottom switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases.

Shut-Down Mode

The JWH5276 operates in shut-down mode when EN is low. In shut-down mode, the entire regulator is off and the supply current consumed by the JWH5276 drops below 3uA.

Power Switches

N-channel MOSFET switches are integrated on the JWH5276 to down convert the input voltage to the regulated output voltage.

Enable and Adjustable VIN UVLO

The EN pin provides electrical on and off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low IQ state. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

For input under-voltage lockout (UVLO), use the EN pin as shown in Figure 1 to set up the UVLO by using a resistive divider connected between Vin and ground, with the central tap connected to EN. Once the EN pin voltage exceeds 1.3 V, an additional 2.95 µA of hysteresis is added. This additional current facilitates input voltage hysteresis. Use Equation 1 and Equation 2 to set the input startup voltage and external hysteresis for the input voltage.

$$R_{EN\_H} = \frac{V_{STR}\left(\frac{V_{EN\_L}}{V_{EN\_H}}\right) - V_{STOP}}{i_p \times \left(1 - \frac{V_{EN\_L}}{V_{EN\_H}}\right) + i_{hy}} \quad (1)$$

$$R_{EN\_L} = \frac{R_{EN\_H} \times V_{EN\_L}}{V_{STOP} - V_{EN\_L} + R_{EN\_H} \times \left(i_p + i_{hy}\right)} \quad (2)$$

where R_{EN_H} and R_{EN_L} are in Ω, i_p=0.55uA, i_{hy}=2.95uA, V_{EN_H}=1.3V and V_{EN_L}=1.18V.

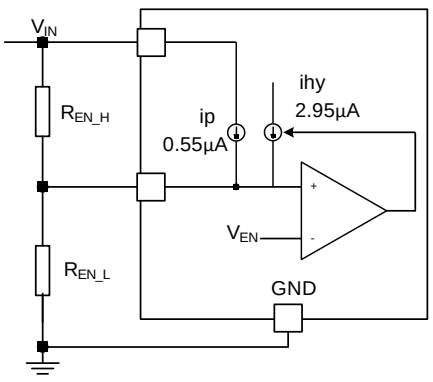

Figure 1. UVLO Setting

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It is recommended that the minimum input shutdown voltage be set at 2.48 V or higher to ensure proper operation before shutdown.

Current Limit and SCP

JWH5276 have protection against heavy load and short circuit events which switch current limits are designed in JWH5276. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM_TOP}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. Only when output current drops below the valley current limit I_{LIM_BOT} can the top power switch be turned on again. When bottom switch current limit is triggered for 4150 consecutive switching cycles, the devices stop switching and discharge the internal soft-start capacitor. The devices then automatically start a new start-up after a typical delay time of 16ms has passed. The devices repeat this mode until the high load condition is removed.

Soft-start

Soft-start is designed in JWH5276 to prevent the converter output voltage from overshooting during startup and short-circuit recovery. An internal current source (I_{SS}) of 2uA is designed to charge the external soft-start capacitor (C_{SS}) and generates a soft-start (SS) voltage ramping up from 0V to 1.8V. When it is less than internal reference voltage ($V_{REF,}$ typ. 0.6V), SS voltage overrides V_{REF} and the error amplifier uses SS voltage as the reference. When SS exceeds V_{REF}, V_{REF} regains control.

T_{SS} can be calculated by the equation 3.

$$T_{SS}(ms) = V_{OUT} \times \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (3)$$

At power up, the soft start pin is discharged before MOSFETs switching to ensure a proper power up. Also, during normal operation, the JWH5276 will stop switching and the soft-start pin will be discharged, when the VIN UVLO is exceeded, EN pin pulled below 1.18V, or a thermal shutdown event occurs.

Output Over-voltage Protection

JWH5276 incorporates an over-voltage transient protection circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVP threshold which is 116.5% of the internal voltage reference. If the FB pin voltage is greater than the OVP threshold, the top switch is disabled preventing current from flowing to the output and minimizing output overshoot. And then the bottom switch is turned-on until its current hit the negative current limit or the FB voltage drops lower than the OVP threshold. When the FB voltage drops lower than the OVP threshold, the top switch is allowed to turn on again.

Adjustable Frequency

The switching frequency of JWH5276 can be programmed by the resistor R_T from the RT pin and GND pin over a wide range from 400 kHz to 2000 kHz. The RT pin voltage is typically 0.5V and must have a resistor to ground to set the switching frequency. The R_T resistance can be estimated by equation 4 for a given switching frequency F_{SW}.

$$R_T(k\Omega) = \frac{57761}{F_{SW}(kHz)^{1.052}} \quad (4)$$

The calculated R_T resistance might need fine-tuning according to bench test. You can also reach to Frequency vs. R_T Resistance Curve in TPC section to find the proper value.

To reduce the solution size one would typically

set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 110 ns which limit the maximum operating frequency in applications with high input to output step down ratios.

Power Good

JWH5276 has a built in power good (PG) function to indicator whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing for multiple rails. The PG pin is an open drain output. It can sink 2mA of current and maintain its specified logic low level.

The PG indicator is in a valid state once the VIN input voltage is greater than 1.2V. JWH5276 features PG=Low when the device is turned-off due to EN UVLO, VIN UVLO or thermal shutdown. After startup, PG is pulled high with a 15μs deglitch time when FB voltage reaches 93.5% of the REF voltage.

When FB voltage drops to 91.5% of the REF voltage, or exceeds 116.5% of the nominal REF voltage, PG is pulled low with a 13us deglitch time.

Thermal Protection

When the temperature of the JWH5276 rises above 170°C, it is forced into thermal shut-down. Only when core temperature drops below 150°C can the regulator becomes active again.

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APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \times \frac{R10}{R9 + R10}$$

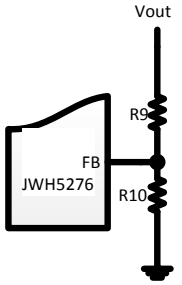
where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R9 around 10KΩ, and then R10 can be calculated by:

$$R10(k\Omega) = \frac{0.6 \times R9}{V_{OUT} - 0.6}$$

The following table lists the recommended values.

VOUT(V)	R9(KΩ)	R10(KΩ)
0.7	10	60
1.2	10	10
2.5	10	3.16
3.3	10	2.2
3.7	10	1.91



Input Capacitor Selection

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{F_{SW} \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value, F_{SW} is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF/0805/6.3V ceramic capacitor is recommended in typical application.

Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_2}\right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system

stability and transient response, and 44uF~88uF ceramic capacitor are recommended in typical application.

Inductor Selection

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

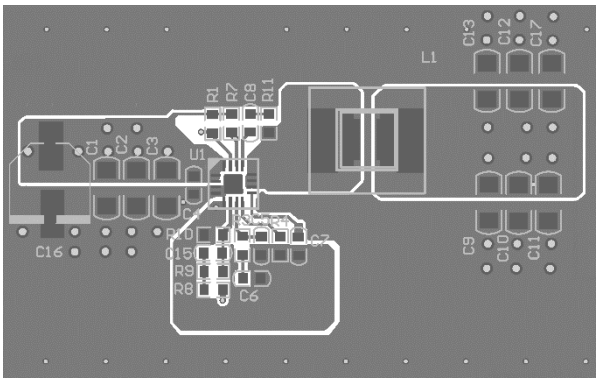
$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, F_{SW} is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

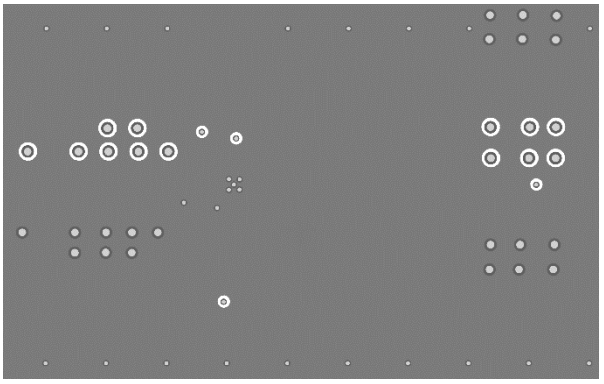
PCB Layout Guidelines (6)

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

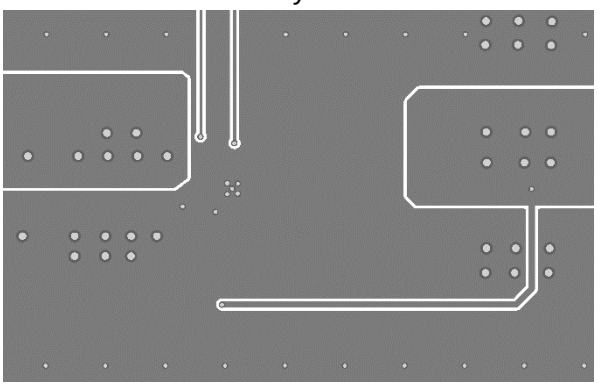
1. Place the input decoupling capacitor as close to JWH5276 (V_{IN} pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling.
5. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.



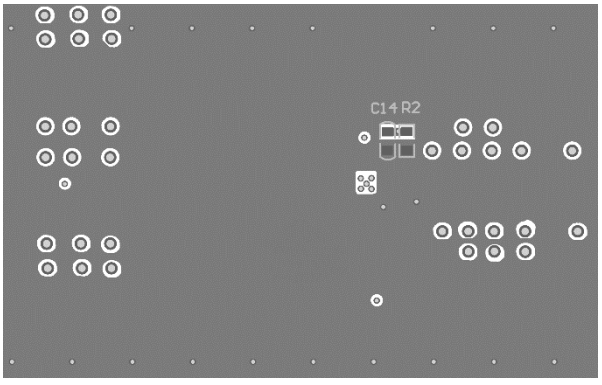
Top and Top Silk Layer



Mid-Layer1



Mid-Layer2



Bottom and Bottom Silk Layer

Notes:

6) The Recommended PCB layout is based on Reference 1

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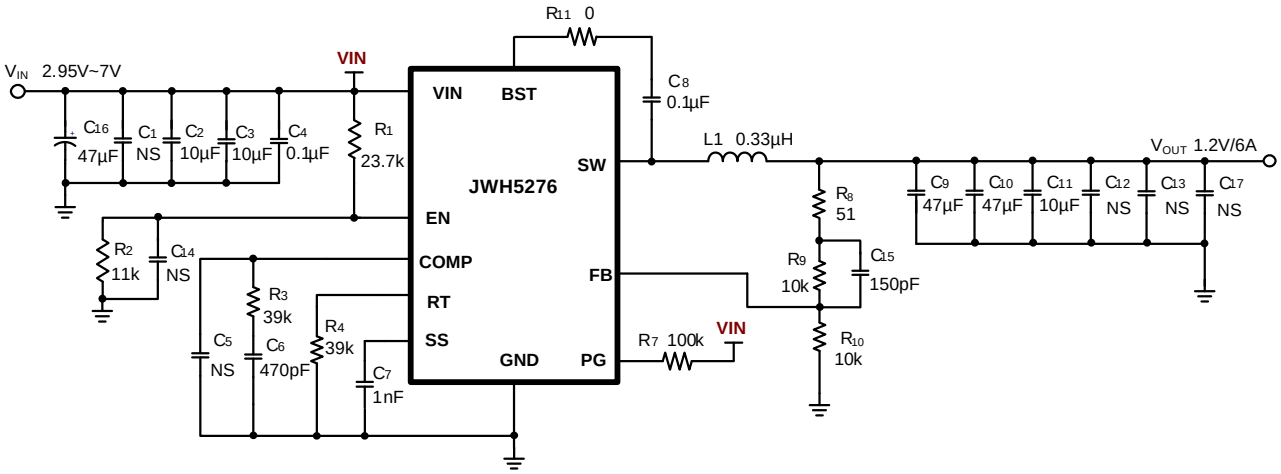
REFERENCE DESIGN

Reference 1:

Vin : 2.95V~7V

Vout: 1.2V

IOUT : 0~6A



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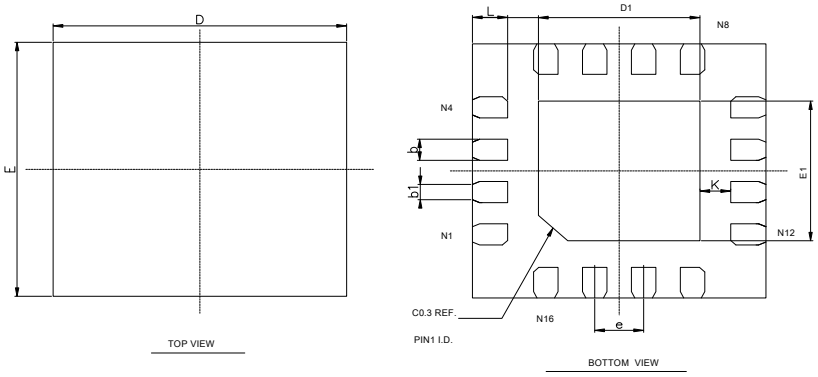
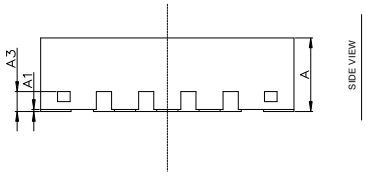
PACKAGE OUTLINE

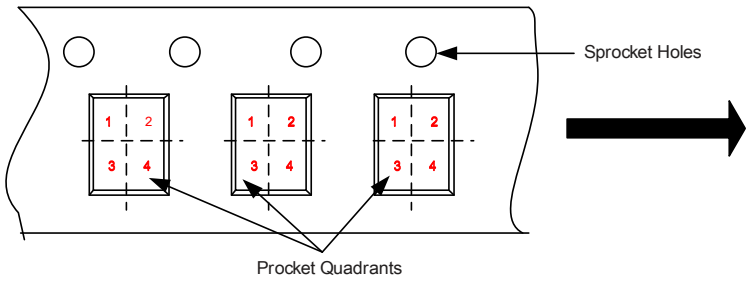
QFN3X3-16 UNIT: mm





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	—	0.05
A3		0.203REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	1.55	1.65	1.75
E1	1.55	1.65	1.75
k		0.315REF	
b	0.20	—	0.30
b1		0.18BCS	
e		0.50BCS	
L	0.26	—	0.46

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
QFN3X3-16	1

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