

*Preliminary Specifications Subject to Change without Notice*

## DESCRIPTION

The JW<sup>®</sup>5352 and JW<sup>®</sup>5352M are monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 4.5V~18V, JW5352 and JW5352M deliver 2A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, JW5352 and JW5352M operate in low frequency to maintain high efficiency.

JW5352 and JW5352M guarantee robustness with output short protection, thermal protection, current run-away protection and input under voltage lockout.

JW5352 and JW5352M are available in SOT23-6 package, which provides a compact solution with minimal external components.

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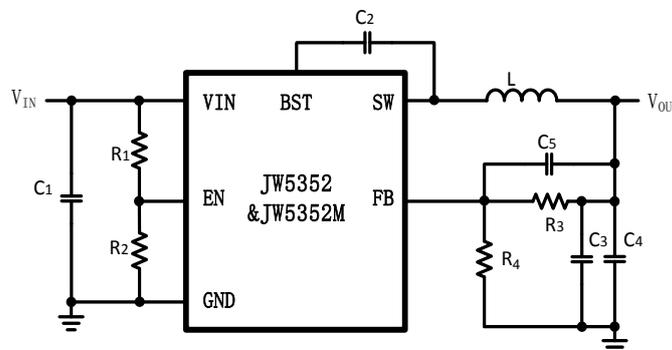
## FEATURES

- 4.5V to 18V operating input range
- 2A output current
- Up to 95% efficiency
- PFM at light load
- 600kHz switching frequency
- Internal soft-start
- Input under-voltage lockout
- Current run-away protection
- Output short protection
- Thermal protection
- Available in SOT23-6 package

## APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

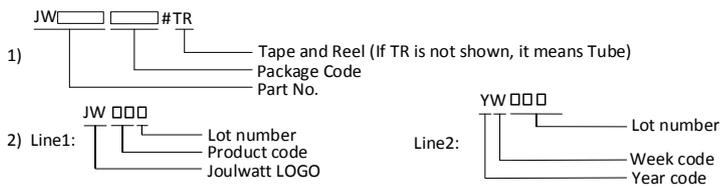
## TYPICAL APPLICATION



**ORDER INFORMATION**

DEVICE <sup>1)</sup>	PACKAGE	TOP MARKING <sup>2)</sup>	ENVIRONMENTAL <sup>3)</sup>
JW5352SOTB#TR	SOT23-6	JWN5□ YW□□□	Green
JW5352MSOTB#TR	SOT23-6	JWN8□ YW□□□	Green

**Notes :**

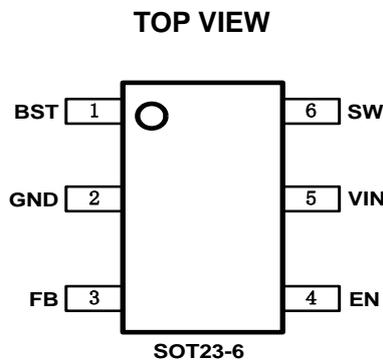


3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

**DEVICE INFORMATION**

DEVICE	Operation Mode at light load	Function	Package	MSL
JW5352SOTB#TR	PFM	-	SOT23-6	MSL1
JW5352MSOTB#TR	PFM	-	SOT23-6	MSL3

**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATING<sup>1)</sup>**

VIN, EN Pin.....	-0.3V to 20V
SW Pin.....	-0.3V(-5V for 10ns) to 20V(22V for 10ns)
BST Pin.....	SW-0.3V to SW+4V
All other Pins .....	-0.3V to 4V
Junction Temperature <sup>2)</sup> .....	150°C
Lead Temperature .....	260°C
Storage Temperature .....	-65°C to +150°C

**RECOMMENDED OPERATING CONDITIONS**

Input Voltage V <sub>IN</sub> .....	4.5V to 18V
Output Voltage V <sub>OUT</sub> .....	0.6V to V <sub>IN</sub> *D <sub>max</sub>
Operation Junction Temperature T <sub>j</sub> .....	-40°C to 125°C

**THERMAL PERFORMANCE**

	$\theta_{JA}$	$\theta_{JC}$
SOT23-6 <sup>3)</sup> .....	220	130°C/W
SOT23-6 <sup>4)</sup> .....	100	25°C/W

**Notes:**

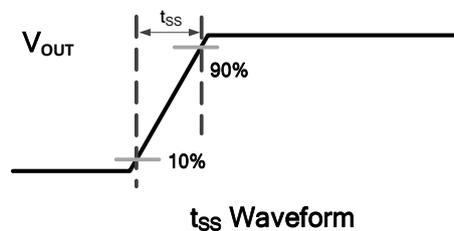
- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The JW5352 and JW5352M include thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) Measured on JESD51-7, 4-layer PCB.
- 4) Measured on a 2OZ two-layer JW5352/JW5352M Evaluation Board at T<sub>A</sub>=25°C.

**ELECTRICAL CHARACTERISTICS**

<i>V<sub>IN</sub>=12V, T<sub>A</sub>=25°C, Unless otherwise stated.</i>						
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub> Under Voltage Lockout Threshold	V <sub>IN_MIN</sub>	V <sub>IN</sub> rising	3.85	4.2	4.45	V
V <sub>IN</sub> Under voltage Lockout Hysteresis	V <sub>IN_MIN_HYST</sub>			300		mV
Shutdown Supply Current	I <sub>SD</sub>	V <sub>EN</sub> =0V		0.1	1	μA
Supply Current	I <sub>Q</sub>	V <sub>EN</sub> =5V, V <sub>FB</sub> =1V		140	200	μA
Feedback Voltage	V <sub>FB</sub>	4.5V<V <sub>IN</sub> <18V	594	600	606	mV
FB Leakage Current	I <sub>FB</sub>	V <sub>FB</sub> =0.85V			100	nA
Top Switch Resistance	R <sub>DS(ON)T</sub>			130		mΩ
Bottom Switch Resistance	R <sub>DS(ON)B</sub>			70		mΩ
Top Switch Leakage Current	I <sub>LEAK_TOP</sub>	V <sub>IN</sub> =18V, V <sub>EN</sub> =0V, V <sub>SW</sub> =0V		0.1	1	μA
Bottom Switch Leakage Current	I <sub>LEAK_BOT</sub>	V <sub>IN</sub> =18, V <sub>EN</sub> =0V, V <sub>SW</sub> =18V		0.1	1	μA
Bottom Switch Current Limit	I <sub>LIM_BOT</sub>		2.2	2.7	3.2	A
Minimum On Time <sup>5)</sup>	T <sub>ON_MIN</sub>			85		ns
Minimum Off Time	T <sub>OFF_MIN</sub>	V <sub>FB</sub> =0.4V		150		ns
Maximum On Time	T <sub>ON_Max</sub>			4		us
EN Rising Threshold	V <sub>EN_H</sub>	V <sub>EN</sub> rising	1.1	1.2	1.3	V
EN Falling Threshold	V <sub>EN_L</sub>	V <sub>EN</sub> falling	0.98	1.05	1.12	V
Soft-Start Period <sup>5)6)</sup>	t <sub>SS</sub>		0.7	1	1.4	ms
Frequency	f <sub>SW</sub>		480	600	720	kHz
Thermal Shutdown <sup>5)</sup>	T <sub>TSD</sub>			160		°C
Thermal Shutdown Hysteresis <sup>5)</sup>	T <sub>TSD_HYST</sub>			20		°C

**Notes :**

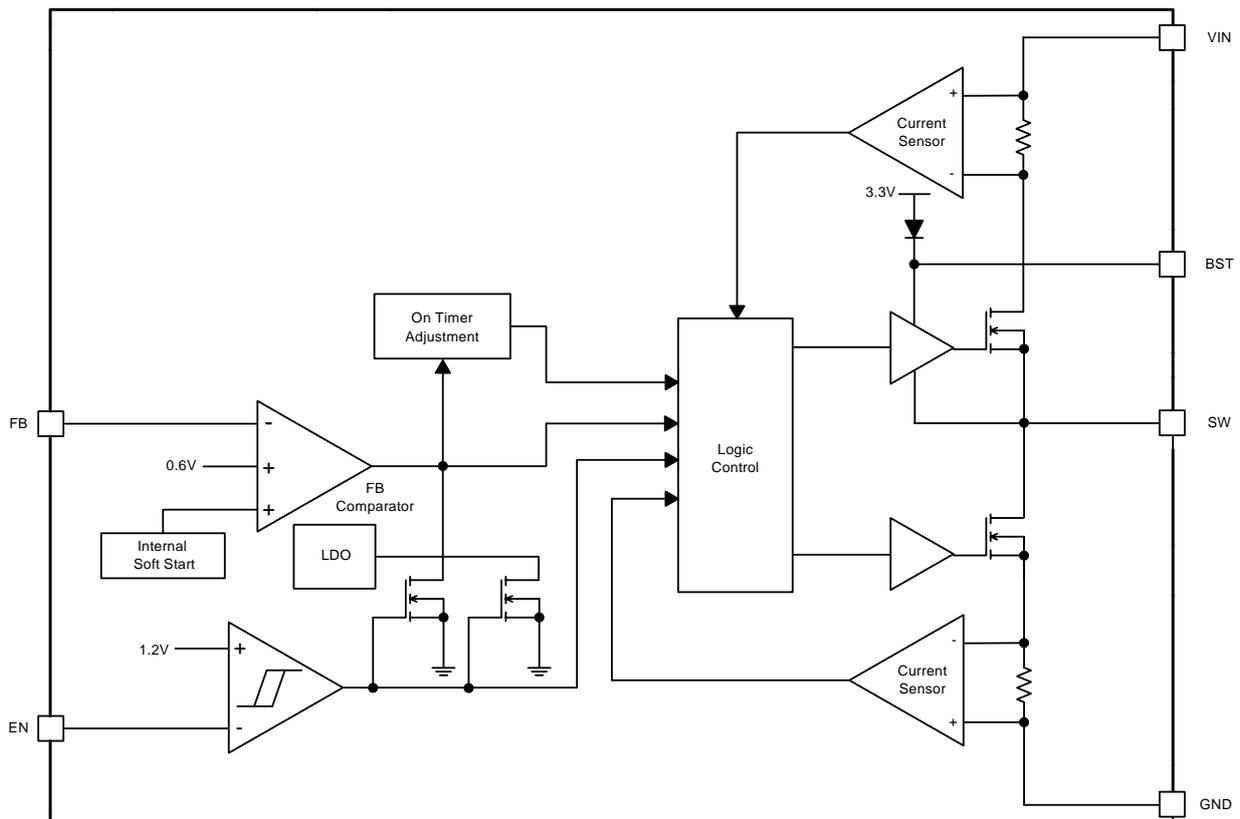
- 5) Guaranteed by design.
- 6) Soft-Start Period is tested from 10% to 90% of the steady state output voltage.



**PIN DESCRIPTION**

SOT23-6	Name	Description
1	BST	Connect a 0.1µF capacitor between BST and SW pin to supply voltage for the top switch driver.
2	GND	Ground pin.
3	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

**BLOCK DIAGRAM**

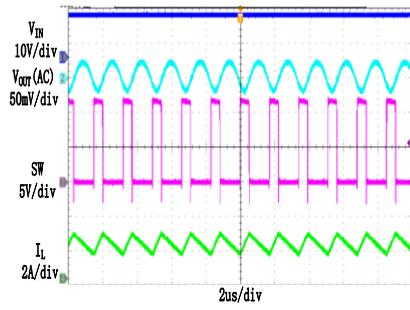


TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $L = 3.3\mu H$ ,  $C_{OUT} = 22\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted

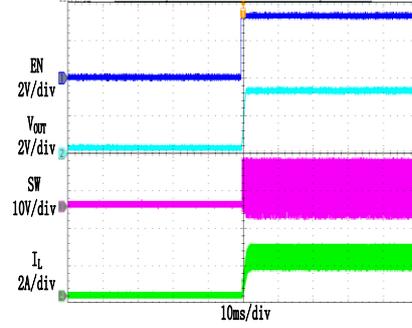
Steady State Test

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$   
 $I_{OUT} = 2A$



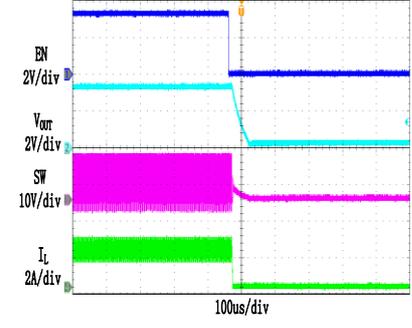
Startup through Enable

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$   
 $I_{OUT} = 2A$  (Resistive load)



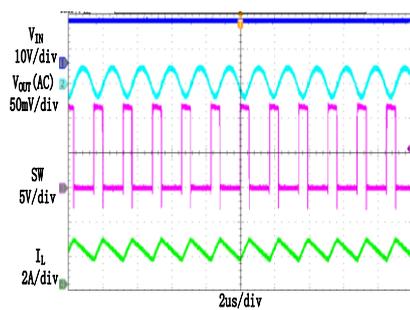
Shutdown through Enable

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$   
 $I_{OUT} = 2A$  (Resistive load)



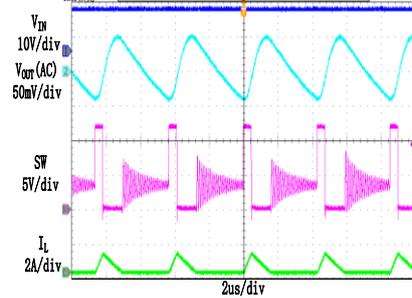
Heavy Load Operation

2A LOAD



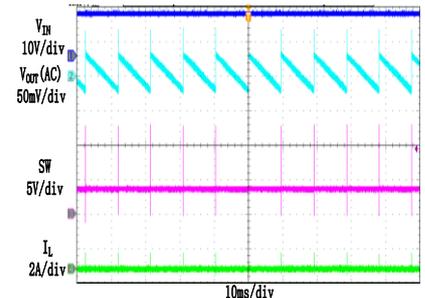
Medium Load Operation

0.2A LOAD



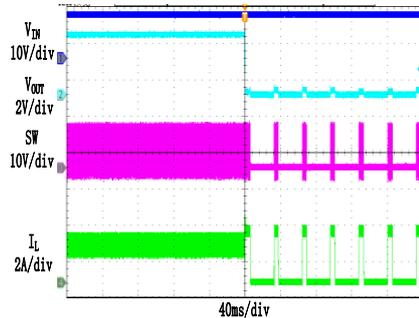
Light Load Operation

0A LOAD



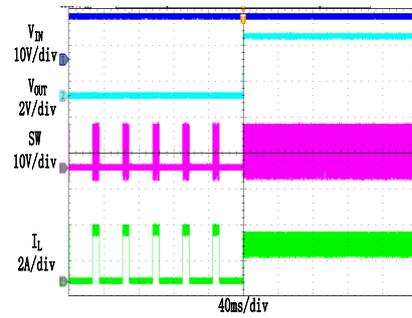
Short Circuit Protection

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$   
 $I_{OUT} = 2A$  - Short



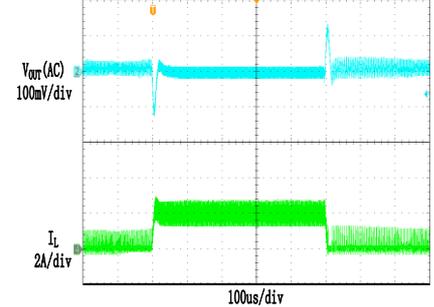
Short Circuit Recovery

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$   
 $I_{OUT} = \text{Short-}2A$



Load Transient

$C_5 = 51pF$   
 0.2A LOAD  $\rightarrow$  2A LOAD  $\rightarrow$  0.2A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS

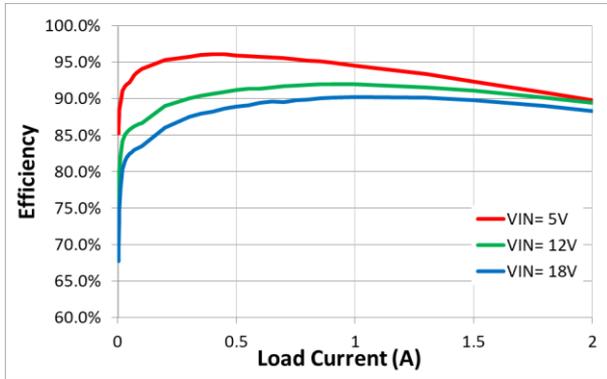


Figure 1. Efficiency vs. Load Current  
( $V_{OUT}=3.3V, L=3.3\mu H$ )

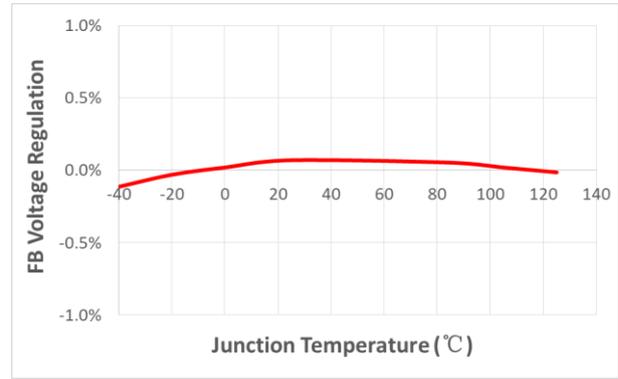


Figure 2. FB Voltage Regulation vs. Junction Temperature

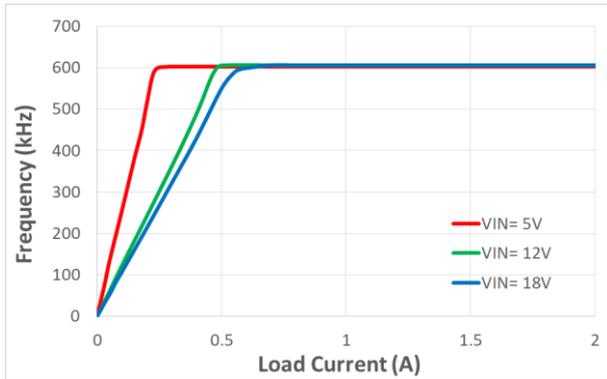


Figure 3. Frequency vs. Load Current  
( $V_{OUT}=3.3V, L=3.3\mu H$ )

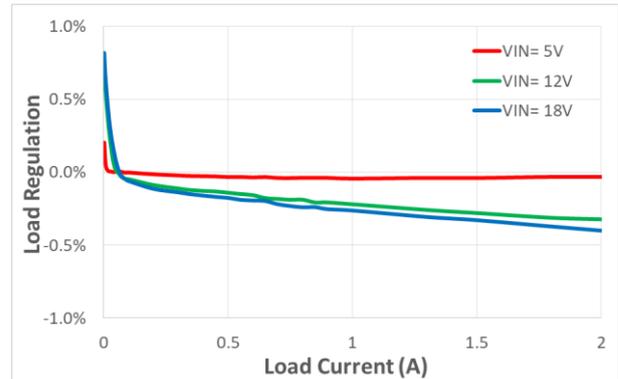


Figure 4. Load Regulation vs. Load Current  
( $V_{OUT}=3.3V, L=3.3\mu H$ )

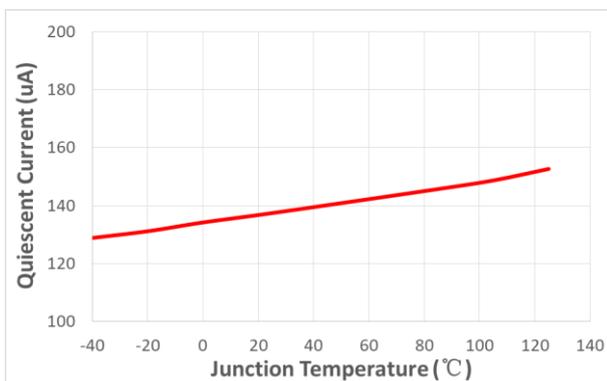


Figure 5. Supply Current vs. Junction Temperature

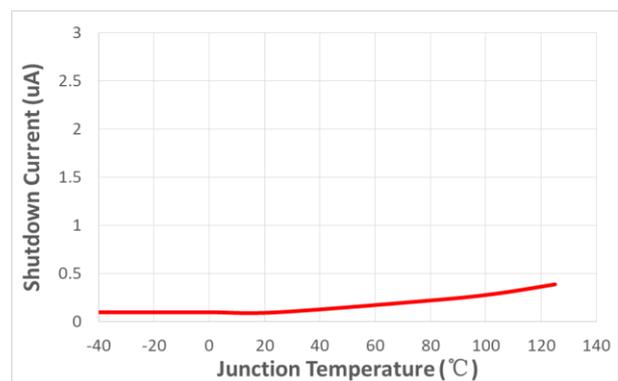


Figure 6. Shutdown Current vs. Junction Temperature

## FUNCTIONAL DESCRIPTION

JW5352 and JW5352M are synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4.5V to 18V down to an output voltage as low as 0.6V, and is capable of supplying up to 2A of load current.

### Shut-Down Mode

The regulator shuts down when voltage at EN pin is driven below 0.4V. The entire regulator is off and the supply current consumed by the regulator drops below 1 $\mu$ A.

### Power Switch

N-Channel MOSFET switches are integrated on the JW5352 and JW5352M to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.3V rail when SW is low.

### CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps.

In CCM operation, the switching frequency is fairly constant; hence the output ripple keeps almost the same.

### PFM Operation

At light load condition, JW5352 and JW5352M are configured to work in PFM mode to optimize the efficiency. When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to PFM mode.

In PFM operation, the high side MOSFET is turned off by the peak current reference and the low side MOSFET turns on until the inductor current reaches zero. At this time, the output voltage is still higher than the target value which causes the internal COMP voltage lower than a clamp value, and the high side MOSFET is not allowed to turn on until the COMP voltage rises above its clamp voltage.

### V<sub>IN</sub> Under-Voltage Protection

A resistive divider can be connected between V<sub>IN</sub> and ground, with the central tap connected to EN, so that when V<sub>IN</sub> drops to the pre-set value, EN drops below 1.05V to trigger input under voltage lockout protection.

### Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current. A valley current limit is designed in JW5352 and JW5352M so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

### Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 2048 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 2048 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 6144 cycles. After the 6144 hiccup cycles, the regulator will try to start-up again. If the short

condition still exists after 2048 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

### **Thermal Protection**

When the temperature of the regulator rises above 160°C, it is forced into thermal shut-down. Only when core temperature drops below 140°C can the regulator become active again.

## APPLICATION INFORMATION

### Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_4}{R_4 + R_3}$$

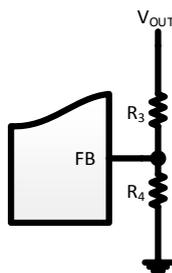
where  $V_{FB}$  is the feedback voltage and  $V_{OUT}$  is the output voltage.

Choose  $R_4$  around 11kΩ, and then  $R_3$  can be calculated by:

$$R_3 = R_4 \cdot \left( \frac{V_{OUT}}{0.6} - 1 \right)$$

The following table lists the recommended values.

$V_{OUT}(V)$	$R_4(k\Omega)$	$R_3(k\Omega)$
0.8	11	3.7
1	11	7.3
1.2	11	11
1.8	11	22
2.5	11	34.8
3.3	11	49.5
5	11	80.7



### Feedforward Capacitor

In order to improve dynamic performance, a feedforward capacitor ( $C_5$ ) can be considered to be in parallel with  $R_3$ .

### Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where  $I_{LOAD}$  is the load current,  $V_{OUT}$  is the output voltage,  $V_{IN}$  is the input voltage.

The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where  $C_1$  is the input capacitance value,  $f_s$  is the switching frequency,  $\Delta V_{IN}$  is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimize the potential noise, a small X5R or X7R ceramic capacitor, e.g. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22μF/25V ceramic capacitor is recommended in typical application.

### Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left( R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_{OUT}} \right)$$

where  $C_{OUT}$  is the output capacitance value and  $R_{ESR}$  is the equivalent series resistance value of

the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, and lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 22µF~44µF ceramic capacitor is recommended in typical application.

**Inductor**

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \cdot \Delta I_L} \cdot \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where  $V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage,  $f_s$  is the switching frequency, and  $\Delta I_L$  is the peak-to-peak inductor ripple current.

**External Bootstrap Capacitor**

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1µF low ESR ceramic capacitor is recommended to be connected between the BST pin and SW pin.

**PCB Layout Note**

For minimum noise problem and best operating performance, the PCB is preferred to follow the guidelines as below.

1. Place the input decoupling capacitor as close to JW5352 or JW5352M (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

SOT23-6:

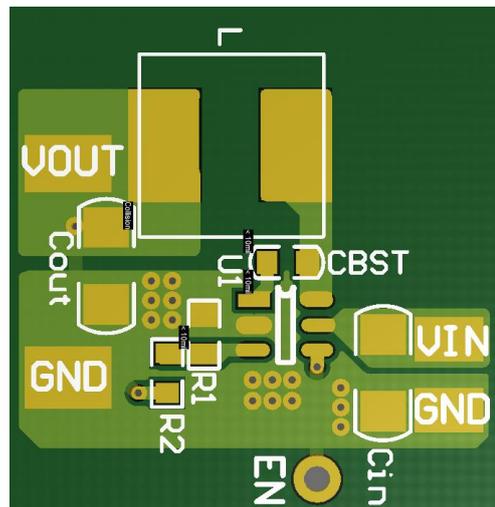


Figure7. PCB Layout Recommendation

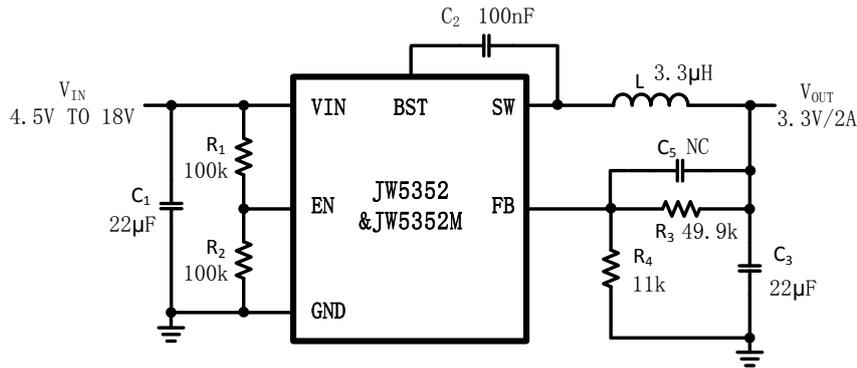
**REFERENCE DESIGN**

**Reference 1:**

$V_{IN}$ : 4.5V~18V

$V_{OUT}$ : 3.3V

$I_{LOAD}$ : 0~2A



**External Components Suggestion ( $V_{IN}=12V$ ):**

$V_{OUT}(V)$	$R_4 (k\Omega)$	$R_3 (k\Omega)$	$C_5 (pF)$	$L (\mu H)$	$C_{3\_MIN} (\mu F)$	$C_{3\_EFF} (\mu F)$
0.8	11	3.7	NC	1.5	44	30
1	11	7.3	NC	2.2	44	30
1.2	11	11	NC	2.2	44	30
1.8	11	22	NC	3.3	32	20
2.5	11	34.8	NC	3.3	22	10
3.3	11	49.5	NC	3.3	22	10
5	11	80.7	NC	4.7	22	10

**Notes:**

- 1) In order to improve dynamic performance, a feedforward capacitor ( $C_5$ ) can be considered to be in parallel with  $R_3$ .
- 2) Capacitor tolerance and bias voltage de-rating should be considered. The effective capacitance can vary by +20% and -80%. Please refer to the datasheet of capacitor.
- 3)  $C_{3\_MIN}$  is the minimum nominal capacitance value of  $C_3$  (output capacitance).  $C_{3\_EFF}$  is the minimum effective capacitance value of  $C_3$ .
- 4) Joulwatt's customers are responsible for determining suitability of components chosen for their purposes. Customers should validate their design implementation to make sure the proper system functionality.

PACKAGE OUTLINE

SOT23-6 UNIT: mm

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	--	1.30
A1	0	0.05	0.15
A2	0.95	1.10	1.20
b	0.30	0.40	0.50
c	0.05	--	0.23
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 (BSC)		
L	0.30	0.45	0.60
θ	0°	—	8°

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Package Type	Pin1 Quadrant
SOT23-6	3

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