

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

The JW[®]5213L is a current mode monolithic buck switching regulator. Operating with an input range of 2.5V-6V, the JW5213L delivers 3A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, the regulator operate in low frequency to maintain high efficiency and low output ripples. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The JW5213L guarantees robustness with latch off output short-circuit protection, latch off over-voltage protection, start-up current run-away protection, input under voltage lockout protection, hot-plug in protection, and thermal protection.

The JW5213L provides output power good indication.

The JW5213L is available in 8-pin DFN2X2-8 package, which provides a compact solution with minimal external components.

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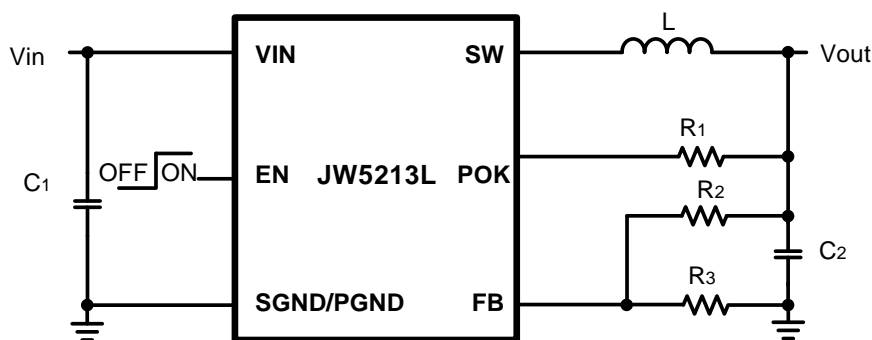
FEATURES

- 2.5V to 6V operating input range
- Up to 3A output current
- Up to 95% peak efficiency
- Internal soft-start
- 1MHz switching frequency
- Input under voltage lockout
- Short circuit protection
- Over voltage protection
- Thermal protection
- Hot-plug in protection
- Output POK indication
- RoHS compliant and halogen free
- Available in DFN2X2-8 package

APPLICATIONS

- 5V or 3.3V Point of Load Conversion
- Set Top Boxes
- Telecom/Networking Systems
- Storage Equipment
- GPU/DDR Power Supply

TYPICAL APPLICATION



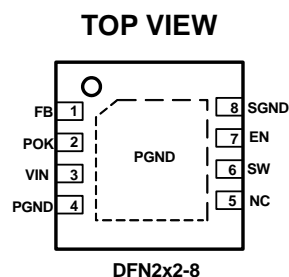
ORDER INFORMATION

DEVICE ¹⁾	PACKAGE	TOP MARKING ²⁾
JW5213LDFND#TRPBF	DFN2X2-8	JWFU□ YW□□□

Notes:

- 1) JW□□□#TRPBF
- JW□□□: PB Free, Tape and Reel (If "TR" is not shown, it means tube)
 - #: Package Code
 - TRPBF: Part No.
- 2) Line1: JW□□□□
- JW□□□□: Internal control code, Product code, Joulwatt LOGO
- Line2: YW□□□□
- YW□□□□: Lot number, Week code, Year code

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATING¹⁾

EN, FB, POK Pins.....	-0.3V to 7.0 V
Vin, SW Pins.....	-0.3V(-1.7V for 20ns) to 7.0V(8.0V for 10ns)
Junction Temperature. ²⁾	150°C
Lead Temperature.....	260°C
Storage Temperature.....	-65°C to +150°C
ESD Susceptibility (Human Body Model)	2kV

RECOMMENDED OPERATING CONDITIONS³⁾

Input Voltage VIN.....	2.5V to 6V
Output Voltage Vout.....	0.6V to Dmax*VIN
Operating Junction Temperature.....	-40°C to 125°C

THERMAL PERFORMANCE⁴⁾
 θ_{JA} θ_{Jc}

DFN2x2-8.....	120...8.2°C/W
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Note:

- 1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
- 2) The JW5213L includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

<i>V_{IN}=5V, T_A=25 °C, unless otherwise stated.</i>						
Item	Symbol	Condition	Min.	Typ.	Max.	Units
V _{IN} Under Voltage Lockout Threshold	V _{IN_UVLO}	V _{IN} rising	2.25	2.4	2.55	V
V _{IN} Under Voltage Lockout Hysteresis	V _{IN_UVLO_HYST}			220		mV
V _{IN} Over Voltage Protection Threshold	V _{IN_OVP}	V _{IN} rising	6.5	6.85	7.2	V
V _{IN} Over Voltage Protection Hysteresis	V _{IN_OVP_HYST}			350		mV
Shutdown Current	I _{SHDN}	V _{EN} =0V		0.1	1	μA
Quiescent Current	I _Q	V _{EN} =2V, V _{FB} =V _{REF} *105%		50	80	μA
Regulated Feedback Voltage	V _{FB}	2.5V<V _{IN} <6V	0.588	0.6	0.612	V
PFET On Resistance	R _{DSON_P}	V _{IN} =3.6V, I _{SW} =200mA		110		mΩ
NFET On Resistance	R _{DSON_N}	V _{IN} =3.6V, I _{SW} =-200mA		90		mΩ
PFET Leakage Current	I _{LEAK_P}	V _{IN} =5.5V, V _{SW} =0V			1	uA
NFET Leakage Current	I _{LEAK_N}	V _{IN} =5.5V, V _{SW} =5.5V			1	uA
PFET Current Limit	I _{LIM_TOP}		3.5	4.8		A
Switching Frequency	F _{SW}	I _{OUT} =1A	0.8	1	1.2	MHz
Minimum On Time ⁵⁾	T _{ON_MIN}			80		ns
Maximum Duty Cycle ⁵⁾	D _{MAX}			75		%
EN Input Logic High Voltage	V _{EN_H}	V _{EN} rising, FB=0.4V	1.15			V
EN Input Logic Low Voltage	V _{EN_L}	V _{EN} falling, FB=0.4V			0.4	V
Short Circuit Protection Threshold ⁵⁾	V _{SCP}			240		mV
POK Lower Low Threshold	V _{POKL_LO}	V _{FB} falling	510	540	570	mV
POK Upper Low Threshold	V _{POKL_UP}	V _{FB} rising	690	720	750	mV
Over-voltage Protection Threshold	V _{OVP}	V _{FB} rising	690	720	750	mV
Over-voltage Deglitch Time	T _{OVP}			30		us
Soft-start Time	t _{ss}	V _{out} from 0% to 95%	0.65		1.08	ms
SW Discharge Resistance	R _{DISC}			50		Ω
Thermal Shutdown Threshold ⁵⁾	T _{SHDN}			150		°C
Temperature Hysteresis ⁵⁾	T _{HYS}			15		°C

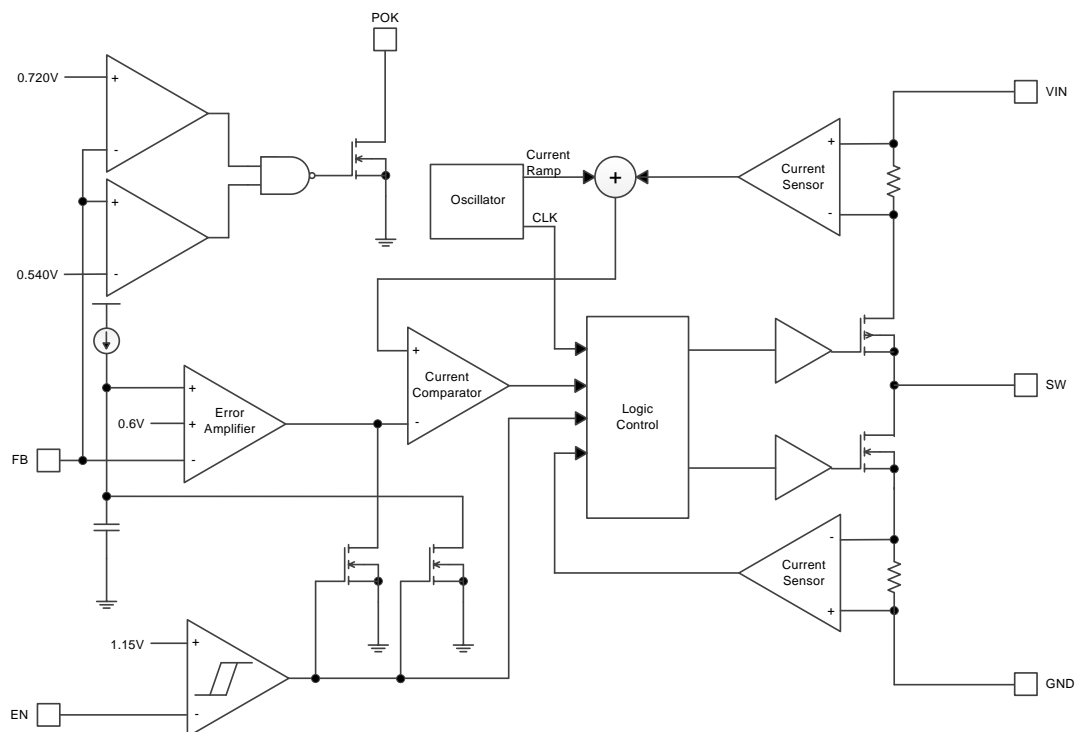
Note:

5) Guaranteed by design.

PIN DESCRIPTION

Pin	Name	Description
1	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
2	POK	Open drain output. Connect a 10K Ω resistor from POK to output. POK is high when V_{FB} is within >90% and <120% of V_{REF} .
3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 2.5V to 6V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	PGND	Power ground pin.
5	NC	No connection.
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
7	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
8	SGND	Signal ground pin.
Exposed Pad	PGND	Power ground pin.

BLOCK DIAGRAM

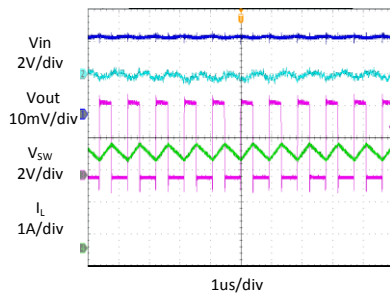


TYPICAL PERFORMANCE CHARACTERISTICS

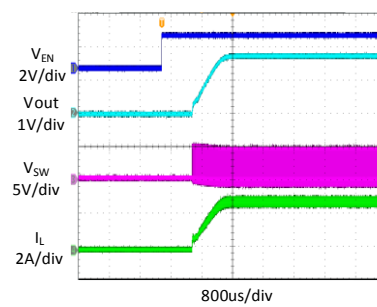
$V_{in} = 5V$, $V_{out} = 1.8V$, $L = 2.2\mu H$, $C_{out} = 44\mu F$, $T_A = +25^\circ C$, unless otherwise noted

Steady State Test

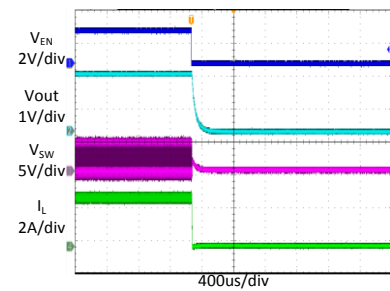
$V_{in}=5V$, $V_{out}=1.8V$
 $I_{out}=3A$

**Startup through Enable**

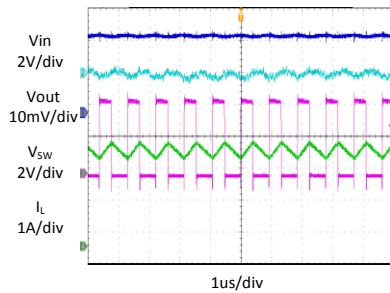
$V_{in}=5V$, $V_{out}=1.8V$
 $I_{out}=3A$ (Resistive load)

**Shutdown through Enable**

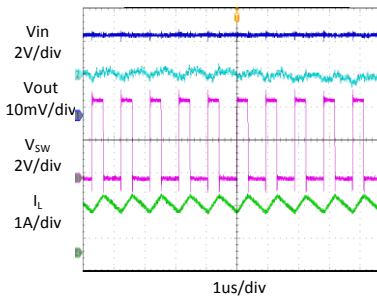
$V_{in}=5V$, $V_{out}=1.8V$
 $I_{out}=3A$ (Resistive load)

**Heavy Load Operation**

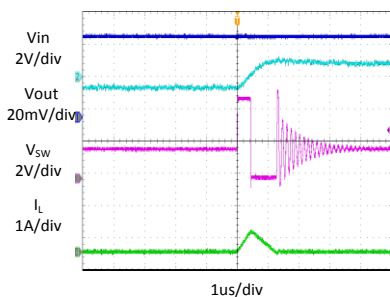
3A LOAD

**Medium Load Operation**

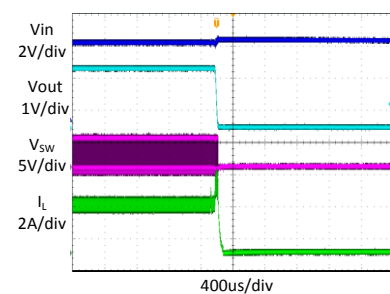
1.5A LOAD

**Light Load Operation**

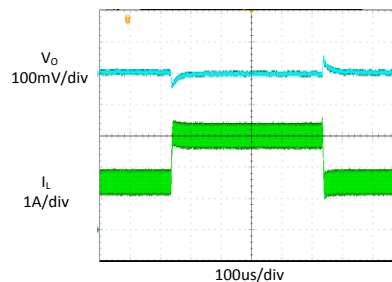
0 A LOAD

**Short Circuit Protection**

$V_{in}=5V$, $V_{out}=1.8V$
 $I_{out}=3A$ - Short

**Load Transient**

1.5A LOAD \rightarrow 3A LOAD
 \rightarrow 1.5A LOAD

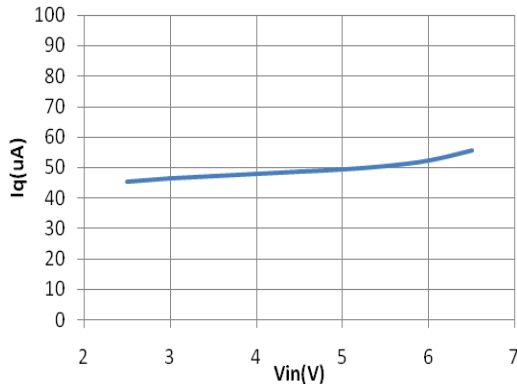


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{in} = 5V$, $V_{out} = 1.8V$, $L = 2.2\mu H$, $C_{out} = 44\mu F$, $T_A = +25^\circ C$, unless otherwise noted

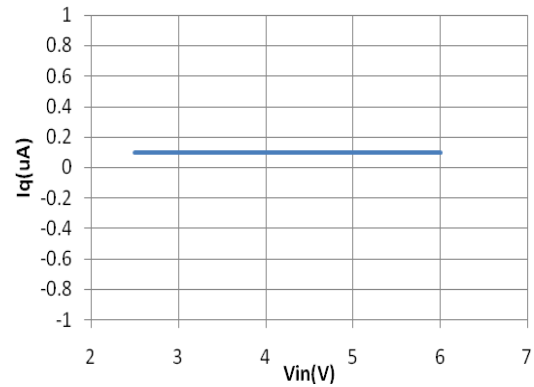
Quiescent Current Vs. Input Voltage

$V_{IN}=3V \sim 6.5V$, $V_{EN}=3V$, $V_{FB}=0.8V$

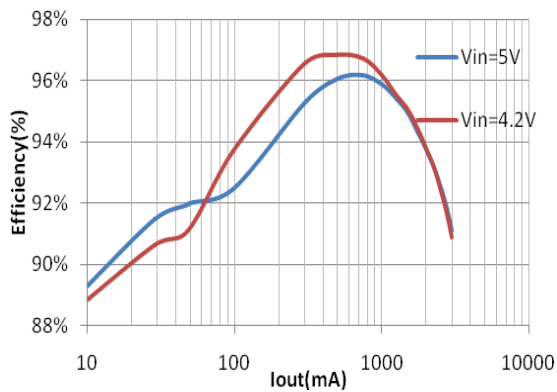


Shutdown Current Vs. Input Voltage

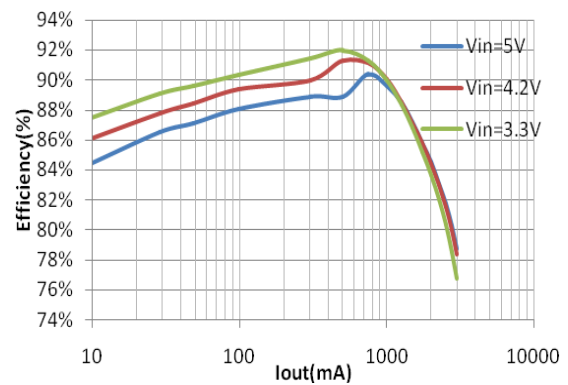
$V_{IN}=3V \sim 6.5V$, $V_{EN}=0V$, $V_{FB}=0.3V$



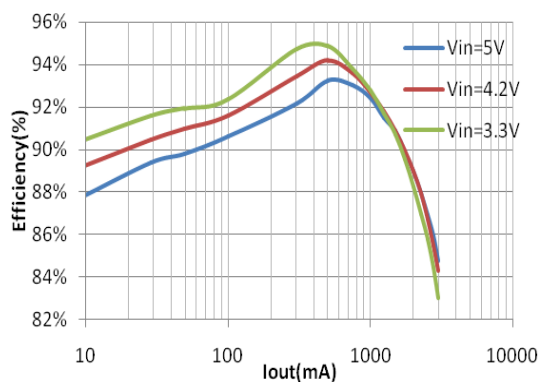
Efficiency @ $V_{out}=3.3V$



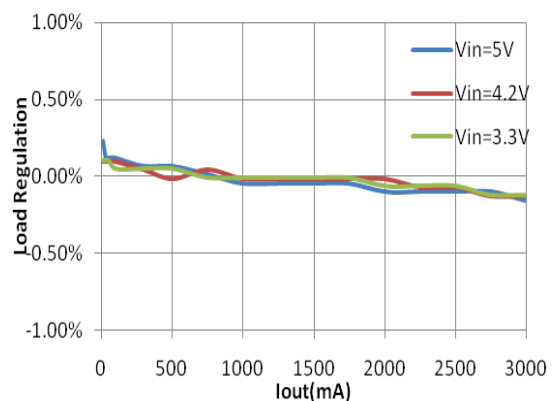
Efficiency @ $V_{out}=1.2V$



Efficiency @ $V_{out}=1.8V$



Load regulation @ $V_{out}=1.8V$



FUNCTIONAL DESCRIPTION

The JW5213L is a synchronous, current-mode, step-down regulator. It regulates input voltages from 2.5V~6V down to an output voltage as low as 0.6V, and is capable of supplying up to 3A of load current.

Current-Mode Control

The JW5213L utilizes current-mode control to regulate the output voltage. The output voltage is measured at the FB pin through a resistive voltage divider and the error is amplified by the internal transconductance error amplifier. Output of the internal error amplifier is compared with the switch current measured internally to control the output current limit.

PFM Mode

The JW5213L operates in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripple.

Shut-Down Mode

The JW5213L operates in shut-down mode when voltage at EN pin is driven below 0.4V. In shut-down mode, the entire regulator is off and the supply current consumed by the JW5213L drops below 1uA.

Power Switches

P-channel and N-channel MOSFET switches are integrated on the JW5213L to down convert the input voltage to the regulated output voltage.

Hot-Plug In Protection

If the Vin voltage exceeds 6.85V, IC will turn off power switch, entering over-voltage protection. It will remain in this state until Vin voltage is less than 6V.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the JW5213L so that only when output current drops below the valley current limit can the bottom power switch be turned off. By such control mechanism, the output current at start-up is well controlled.

Short Circuit Protection

When output falls below 40% of the regulation, IC will shut down and enter short circuit protection. Short circuit protection will be removed by Vin or EN restart.

Over voltage protection

IC will shut down and enter overvoltage protection when output voltage is higher than 120% of regulation level for more than 20us. Output voltage will discharge by internal resistor. Overvoltage protection will be removed by Vin or EN restart.

Thermal Protection

When the temperature of the JW5213L rises above 150°C, it is forced into thermal shut-down. Only when core temperature drops below 135°C can the regulator becomes active again.

APPLICATION INFORMATION

Duty Cycle Limit

The JW5213L do not support to work more than 75% duty cycle. The input and output voltages should meet the following condition:

$$D = \frac{V_{OUT}}{V_{IN}} \leq 75\%$$

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_3}{R_2 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_3 around 10K Ω , and then R_2 can be calculated by:

$$R_2 = R_3 \cdot \left(\frac{V_{OUT}}{0.6V} - 1 \right)$$

The following table lists the recommended values.

V _{OUT} (V)	R ₂ (K Ω)	R ₃ (K Ω)
1.2	10	10
1.5	15	10
1.8	20	10
3.3	49.9	11

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_1 is the input capacitance value, f_s is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1 μ F, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22 μ F/0805/10V ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_2} \right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and two 22 μ F/0805/6.3V ceramic capacitors are recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 30% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5213L (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

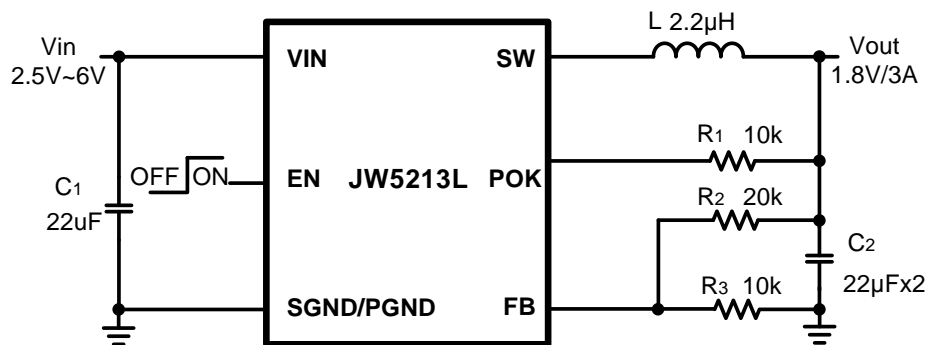
REFERENCE DESIGN

Reference 1:

V_{IN} : 2.5V ~ 6V

V_{OUT} : 1.8V

I_{OUT} : 0~3A

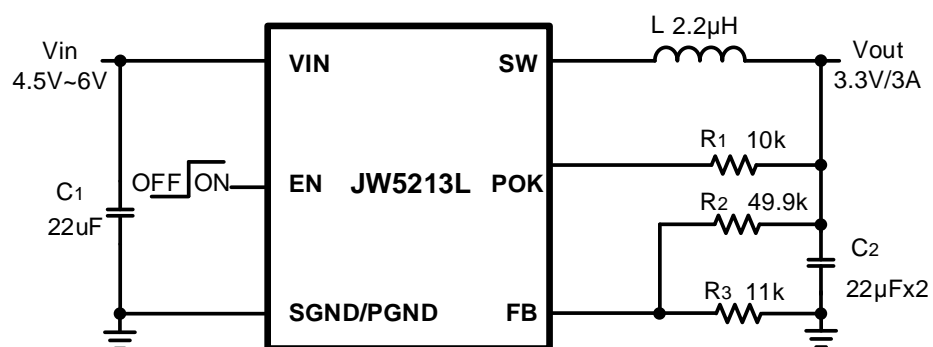


Reference 2:

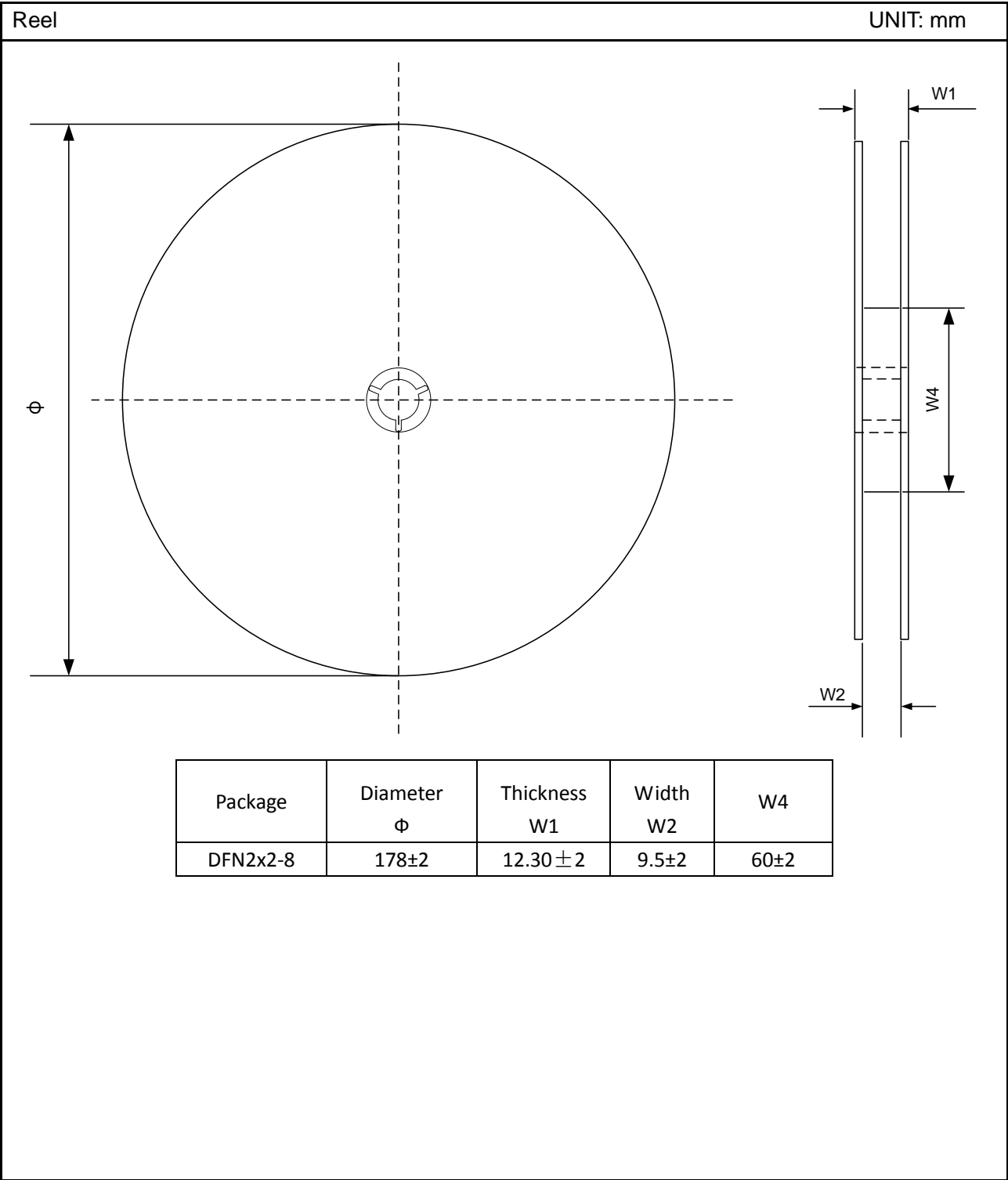
V_{IN} : 4.5V ~ 6 V

V_{OUT} : 3.3V

I_{OUT} : 0~3A

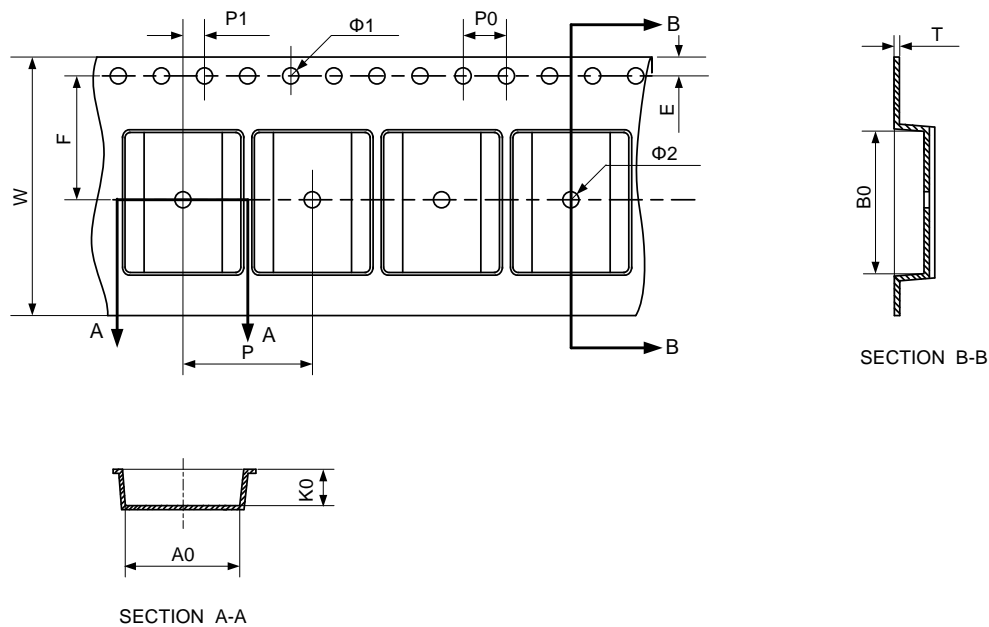


TAPE AND REEL INFORMATION



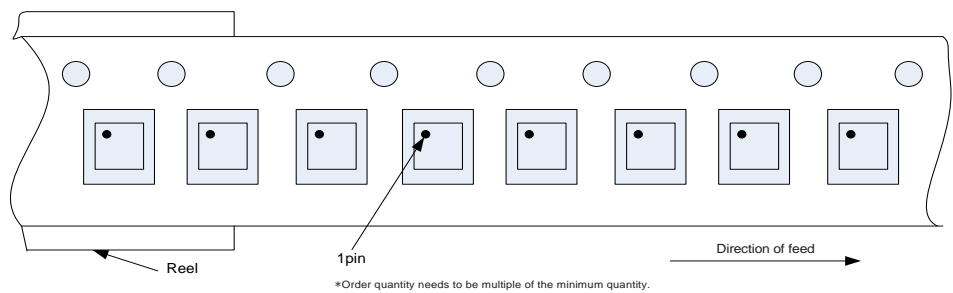
Carrier Tape

UNIT: mm

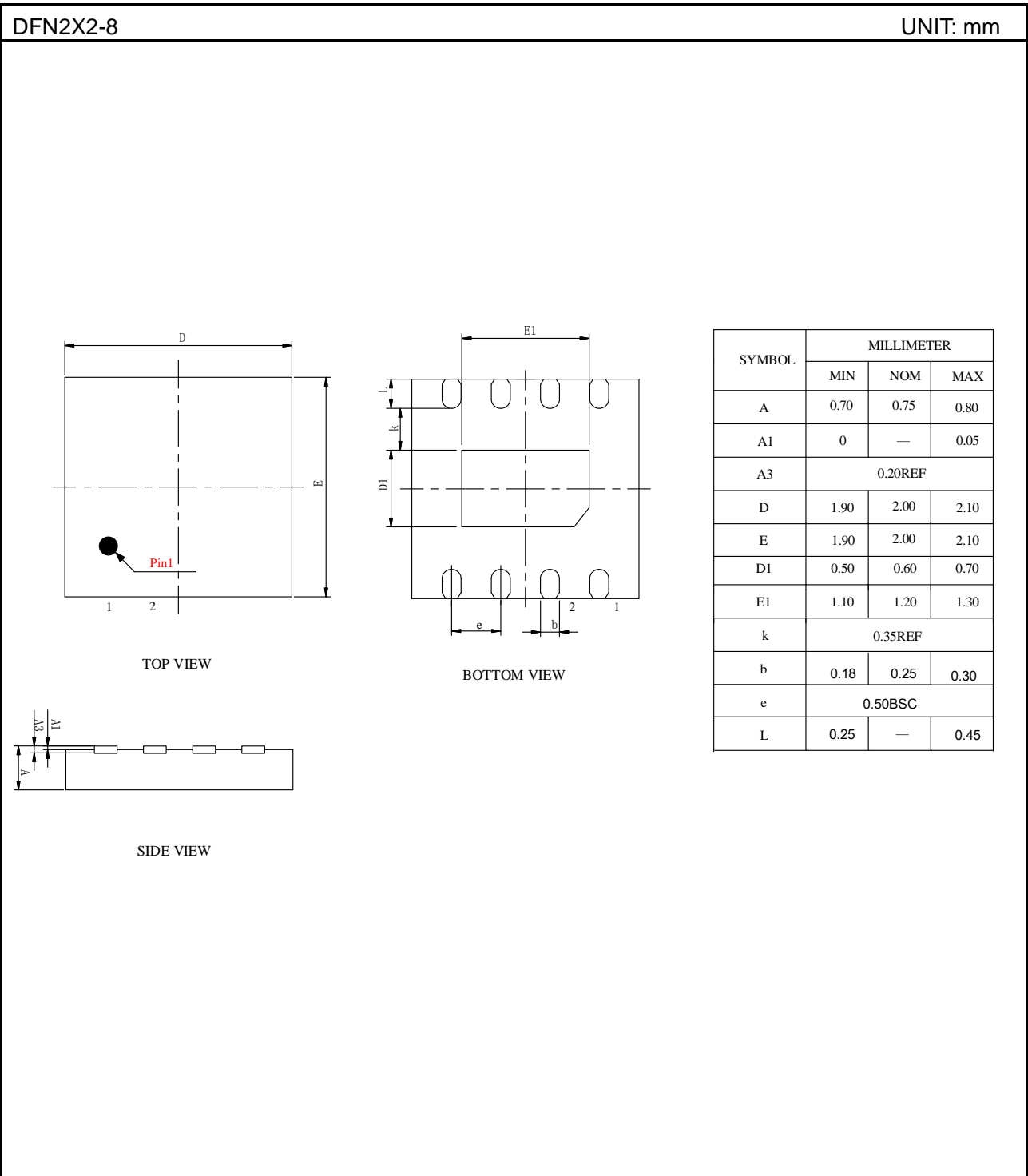


- Note :
- 1) The carrier type is black, and colorless transparent.
 - 2) Carrier camber is within 1mm in 100mm.
 - 3) 10 pocket hole pitch cumulative tolerance: ± 0.20 .
 - 4) All dimensions are in mm.

Package ^①	P0 ^②	P1 ^③	P ^④	A0 ^⑤	B0 ^⑥	W ^⑦	T0 ^⑧	K0 ^⑨	Φ 1 ^⑩	Φ 2 ^⑪	E ^⑫	F ^⑬
DFN 2x2-8 ^①	4.00±0.10 ^②	2.00±0.10 ^③	4.00±0.10 ^④	2.30±0.20 ^⑤	2.30±0.20 ^⑥	8.00±0.30 ^⑦	0.25±0.20 ^⑧	1.00±0.35 ^⑨	1.50min ^⑩	1.00min ^⑪	1.75±0.10 ^⑫	3.50±0.10 ^⑬



PACKAGE OUTLINE



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