# JW7105/JW7105A

## Current-Limit Programmable USB Switch

*Parameters Subject to Change Without Notice*

## DESCRIPTION

The JW®7105/JW7105A is a current-limited programmable USB switches optimized for applications that require precise current limit, or to provide up to 2.4A of continuous load current during heavy loads/short circuits. These devices offer a programmable current-limit threshold between 550mA and 2.4A (Typ.) by an external resistor. The rise and fall times are controlled to minimize current overshoot or undershoot during switches on/off.

The device has fast short-circuit response time for improved overall system robustness. It provides a complete protection solutions, such as over-current protection, over-temperature protection and short-circuit protection, as well as controlled rise time and under-voltage lockout function. A7.5ms deglitch time on the open-drain Flag output prevents false over-current reporting.

JW7105/JW7105A offers SOT23-5 packages.



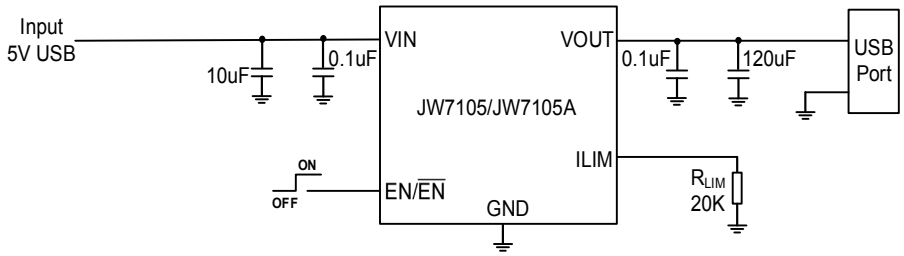
## FEATURES

- Up to 2.4A Maximum Load Current
- Accurate Programmable Current Limit, 550mA-2.4A
- JW7105:EN active high
  JW7105A:EN active low
- Constant-Current During Over-Current
- Fast Short-Circuit Response Time: 2μs (typ.)
- Operating Range: 2.7V - 5.5V
- Built-in Soft-Start with 3ms Typical Rise Time
- Over-Current, and Thermal Protection
- ESD Protection: 2kV HBM, 500V CDM
- Available in SOT23-5Packages

## APPLICATIONS

- Set-Top Boxes
- LCD TVs & Monitors
- Residential Gateways
- Laptops, Desktops, Servers, e-books, Printers, Docking
- Stations, HUBs

## TYPICAL APPLICATION



## ORDER INFORMATION

| DEVICE[1)] | PACKAGE | TOP MARKING[2)] |
|---|---|---|
| JW7105SOTA#TRPBF | SOT23-5 | JWKEX<br>YWLLL |
| JW7105ASOTA#TRPBF | SOT23-5 | JWKFX<br>YWLLL |

**Notes:**

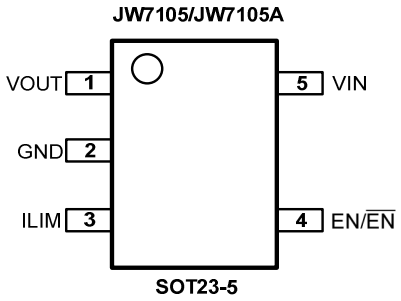
1) JW□□□□# TRPBF
- PB Free
- Tape and Reel(If" TR" is not shown, it means tube)
- Package Code
- Part No.

2) Line1: JWPNA
- Assembly House code
- Product code of JWXXXX
- Joulwatt LOGO

Line2: YWLLL
- Lot number
- Week code
- Year code

## PIN CONFIGURATION

**TOP VIEW**




## ABSOLUTE MAXIMUM RATING[1)]

VIN PIN Voltage ..... -0.3V to 6.5V
VOUTPIN Voltage.....-0.3V to 6.5V
ENPin Voltage.....-0.3V to6.5V
ILIM Source Current.....1mA
JunctionTemperature[2) 3)] .....150ºC
Lead Temperature .....260ºC
Storage Temperature .....-65ºC to +150ºC

## RECOMMENDED OPERATING CONDITIONS

VIN PIN Voltage ..... 2.7V to 5.5V
VOUTPIN Voltage.....0V to (VIN+0.2V)V
EN/$\overline{EN}$PIN Voltage.....0V to 5.5V
High-Level Input Voltage on EN/$\overline{EN}$.....1.4V to VIN

Low-Level Input Voltage on EN/$\overline{EN}$.....0V to 0.5V
Operating Junction Temperature….....-40ºC to 125ºC

## THERMAL PERFORMANCE[4)]

| | $\theta_{JA}$ | $\theta_{Jc}$ |
|---|---|---|
| SOT23-5 | 220 | 130ºC/W |

**Note：**

**1)** Exceeding these ratings may damage the device.

**2)** The JW7105/JW7105A guarantees robust performance from -40°Cto 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

**3)** The JW7105/JW7105A includes thermal protection that is intended to protect the device in overload conditions.

**4)** Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

*TA = +25°C, VIN = 2.7V to 5.5V, $V_{EN}$ = 0V or $V_{EN}$ = VIN, unless otherwise stated.*

| Item | | Symbol | Condition[5] | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| *Supply* | | | | | | | | |
| Input UVLO | | $V_{UVLO}$ | VIN Rising | | | 2.4 | 2.65 | V |
| Input UVLO Hysteresis | | $\Delta V_{UVLO}$ | VIN Decreasing | | | 150 | | mV |
| Input Shutdown Current | | $I_{SHDN}$ | VIN= 5.5V, Disabled, VOUT = Open | | | 0.1 | 1 | uA |
| Input Quiescent Current | | $I_Q$ | VIN= 5.5V, Enabled, VOUT = Open, $R_{LIM}$ = 20kΩ | | | 130 | 160 | uA |
| *Power Switch* | | | | | | | | |
| Switch On-Resistance | | $R_{DS(ON)}$ | SOT23-5 | $T_J$ = +25°C, VIN= 5.0V | | 55 | 65 | mΩ |
| | | | | -40°C ≤ $T_A$ ≤ +85°C | | | 70 | |
| Output Turn-On Rise Time | | $t_R$ | VIN= 5.5V, $C_L$ = 1μF, $R_{LOAD}$ = 100Ω. See Figure 1. | | | 1.1 | 1.5 | ms |
| | | | VIN= 2.7V, $C_L$ = 1μF, $R_{LOAD}$ = 100Ω. | | | 0.7 | 1 | |
| Output Turn-Off Fall Time | | $t_F$ | VIN= 5.5V, $C_L$ = 1μF, $R_{LOAD}$ = 100Ω. See Figure 1. | | 0.1 | | 0.5 | ms |
| | | | VIN= 2.7V, $C_L$ = 1μF, $R_{LOAD}$ = 100Ω. | | 0.1 | | 0.5 | |
| *Current Limit* | | | | | | | | |
| Current-Limit Threshold (maximum DC output current), VOUT = VIN -0.5V | | $I_{LIMIT}$ | $R_{LIM}$ = 10kΩ | -40°C ≤ $T_A$ ≤+85°C | 2.2 | 2.4 | 2.6 | A |
| | | | $R_{LIM}$ = 15kΩ | -40°C ≤ $T_A$ ≤+85°C | 1.4 | 1.6 | 1.8 | |
| | | | $R_{LIM}$ = 20kΩ | -40°C ≤ $T_A$ ≤+85°C | 1.0 | 1.2 | 1.4 | |
| | | | $R_{LIM}$ = 50kΩ | -40°C ≤ $T_A$ ≤+85°C | 0.45 | 0.55 | 0.7 | |
| | | | $I_{LIMIT}$Shorted to GND | | 2.2 | 2.4 | 2.6 | |
| Short-Circuit Current Limit, VOUT Connected to GND | | $I_{SHORT}$ | $R_{LIM}$ = 10kΩ | | | 2.5 | | A |
| | | | $R_{LIM}$ = 15kΩ | | | 1.7 | | |
| | | | $R_{LIM}$ = 20kΩ | | | 1.3 | | |
| | | | $R_{LIM}$ = 49.9kΩ | | | 0.57 | | |
| Short-Circuit Response Time | | $t_{SHORT}$ | VOUT= 0V to $I_{OUT}$ = $I_{LIMIT}$(VOUT shorted to ground). See Figure 2. | | | 2 | | μs |
| *Enable Pin* | | | | | | | | |
| EN/$\overline{EN}$Input Leakage Current | | $I_{LEAK-EN}$ | VIN= 5V, $V_{EN}$ = 0V and 6V | | -0.5 | | 0.5 | uA |
| Turn-On Time | | $t_{ON}$ | $C_L$ = 1μF, $R_L$ = 100Ω.See Figure 1. | | | | 3 | ms |
| Turn-Off Time | | $t_{OFF}$ | $C_L$ = 1μF, $R_L$ = 100Ω.See Figure 1. | | | | 1 | ms |
| JW7105 | EN High Level Voltage | $V_{ENH}$ | | | 1.4 | | | V |
| | EN Low Level Voltage | $V_{ENL}$ | | | | | 1 | V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| JW7105A | EN High Level Voltage | $V_{ENH}$ | | 1.1 | | | V |
| | EN Low Level Voltage | $V_{ENL}$ | | | | 0.7 | V |
| *Output Discharge* | | | | | | | |
| Discharge Resistance[6)] | | $R_{DIS}$ | VIN= 5V, Disabled, $I_{OUT}$ =1mA | | 600 | | Ω |
| *Thermal Shutdown* | | | | | | | |
| Thermal Shutdown Threshold | | $T_{SHDN}$ | Enabled, $R_{LOAD}$ = 1kΩ | | 160 | | °C |
| Thermal Shutdown Threshold underCurrent Limit | | $T_{SHDN\_OCP}$ | Enabled, $R_{LOAD}$ = 1kΩ | | 140 | | °C |
| Thermal Shutdown Hysteresis | | $T_{HYS}$ | | | 20 | | °C |

## Note：

**5)** Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

**6)** The discharge function is active when the device is disabled (when enable is de-asserted or during power-up power-down when VIN< VUVLO).The discharge function offers a resistive discharge path for the external storage capacitor for limited time.

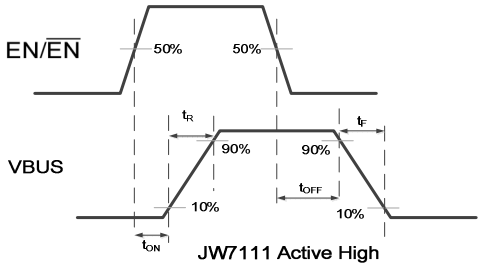
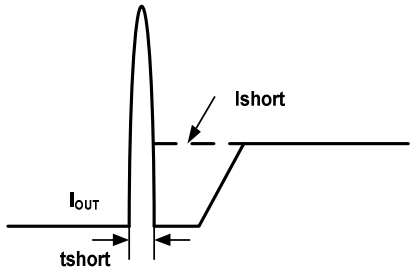



Figure 1 Voltage WaveformsFigure

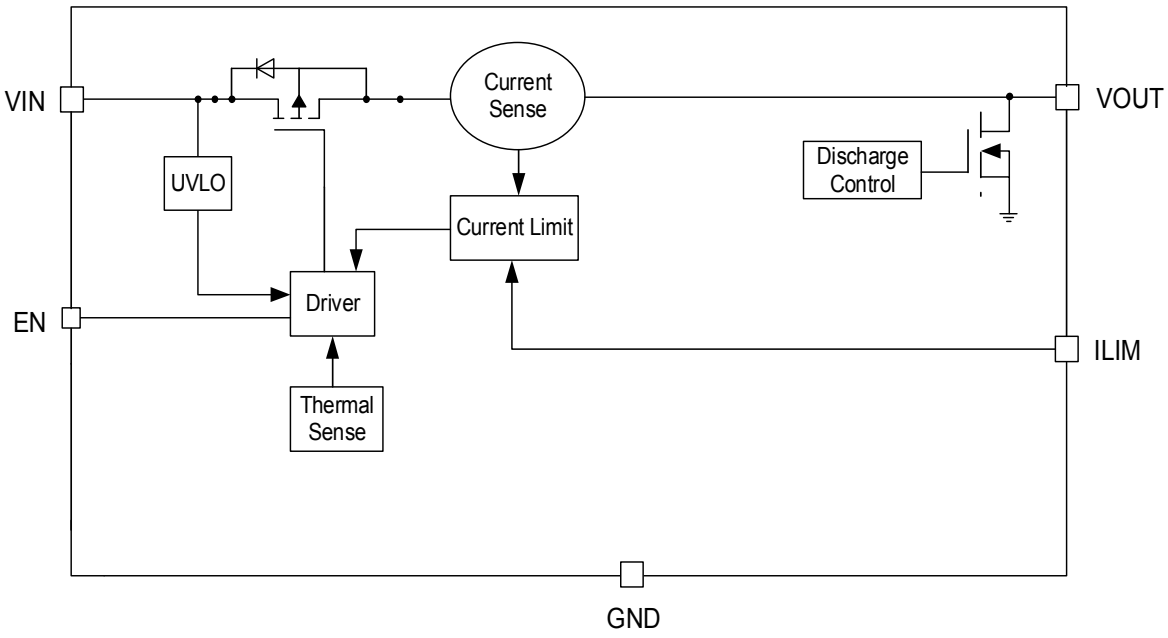



2 Response Time to Short Circuit Waveform

## PIN DESCRIPTION

| Pin SOT23-5 | Name | Description |
|---|---|---|
| 1 | VOUT | Output. |
| 2 | GND | Ground. |
| 3 | ILIM | Use external resistor to set current-limit threshold; Recommended 10kΩ≦ $R_{LIM}$≦49.9kΩ. |
| 4 | EN/$\overline{EN}$ | Enable input.<br>JW7105: logic high turns on power switch.<br>JW7105A: logic low turns on power switch. |
| 5 | VIN | Input, connect a 0.1μF or greater ceramic capacitor from VIN to GND as close to IC as possible. |

## BLOCK DIAGRAM



# FUNCTIONAL DESCRIPTION

The JW7105/JW7105A integrates high-side MOSFET optimized for Universal Serial Bus (USB) that requires protection functions. The MOSFET is driven with controlled gate voltage and slew-rate, which makes this USB device ideal for hot-swap or hot-plug applications.

## Discharge Function

When enable is de-asserted, or when the input voltage is under UVLO level, the discharge function is active. The output capacitor is discharged through an internal NMOS in series with a 100Ω resistor. The discharge time is dependent on the RC time constant of the resistance and output capacitance.

## Power Supply Considerations

A 10μF X7R or X5R ceramic capacitor between VIN and GND, close to the device, is highly recommended. This limits the input voltage drop during line transients. Placing a high-value electrolytic capacitor on the input (10μF minimum) and output pin (120μF) is recommended when the output load is heavy.

Additionally, bypassing the device output with a 0.1μF to 4.7μF ceramic capacitor improves the immunity of the device to short-circuit condition.
This capacitor also prevents output from going negative during turn-off due to parasitic inductance. If the negative kick is less than -1V, a schottky diode in parallel with VOUT pin is recommended. Otherwise, the device may go malfunction.

## Generic Hot-Plug Applications

In many applications it is common to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges. The most effective way to control the current surge is to limit and slowly ramp the current and voltage being applied to the card, similar to the Soft Start in which a power supply normally turns on. Due to the controlled rise and fall times of the JW7105/JW7105A, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system.

The UVLO feature of the JW7105/JW7105A also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

## Generic Hot-Plug Applications

By placing the JW7105/JW7105A between the VCC input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism
for any device.

## Under-Voltage Lockout (UVLO)

Whenever the input voltage falls below UVLO threshold (~2.5V), the power switch is turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

## Over-Current and Short-Circuit Protection

An internal sensing FET is employed to sense over-current conditions. Unlike current-sense resistors, sensing FETs do not increase the series resistance of the current path. When an over current condition is detected, JW7105/JW7105A maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate over-temperature

protection.

## Current Limit Setting

The current limit can be programmed by an external resistor. The current limit is proportional to the current sourced out of ILIM pin.

The recommended 1% resistor range for $R_{LIM}$ is 10kΩ ≤RLIM≤49.9kΩ. The traces routing the $R_{LIM}$ resistor to the JW7105/JW7105A should be as short as possible to reduce parasitic effects on the current-limit accuracy.

To design a maximum current limit, find the intersection of $R_{LIM}$ and the maximum desired load current. The typical current limit can be calculated by

$$I_{lim} = \frac{0.1}{R_{Lim}} \times 232.33 + 0.77$$

And also $R_{LIM}$ can be calculated by

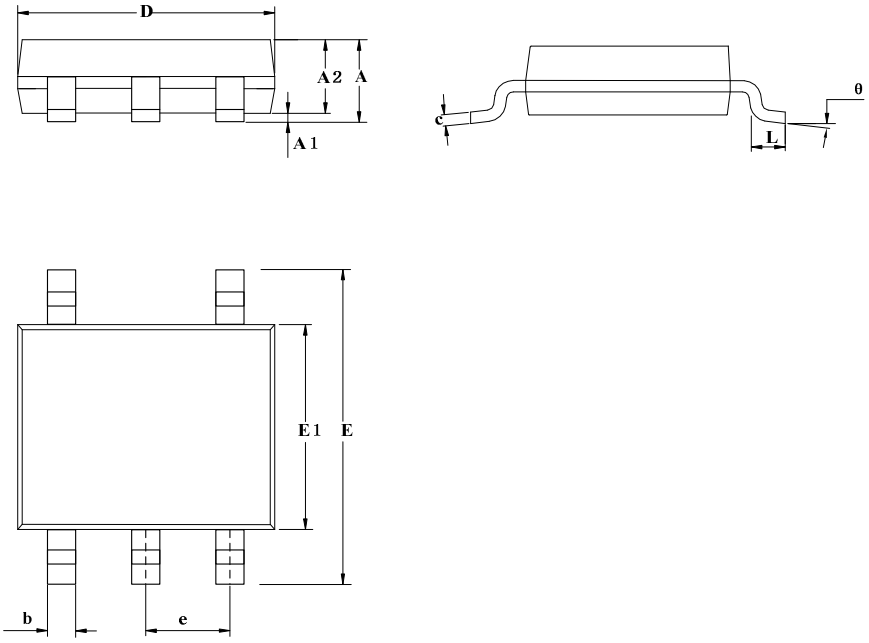
$$R_{lim} = \frac{23.233}{I_{Lim} - 0.77} (k\Omega)$$

## Over-Temperature Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults occurs. The JW7105/JW7105A implements a thermal sensing circuit to monitor the operating junction temperature. Once the die temperature rises to approximately +160°C (+140°C in case the part is under current limit), the thermal protection feature activates as follows: The internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Once the junction temperature drops to 140°C, the MOSFET restart to work.

## PACKAGE OUTLINE

SOT23-5 UNIT: mm




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 1.05 | 1.15 | 1.25 |
| A1 | 0 | 0.05 | 0.15 |
| A2 | 0.95 | 1.05 | 1.20 |
| b | 0.20 | 0.40 | 0.60 |
| c | 0.05 | — | 0.21 |
| D | 2.72 | 2.92 | 3.12 |
| E | 2.60 | 2.80 | 3.00 |
| E1 | 1.40 | 1.60 | 1.80 |
| e | 0.95（BSC） | | |
| L | 0.30 | 0.45 | 0.60 |
| θ | 0° | — | 8° |

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